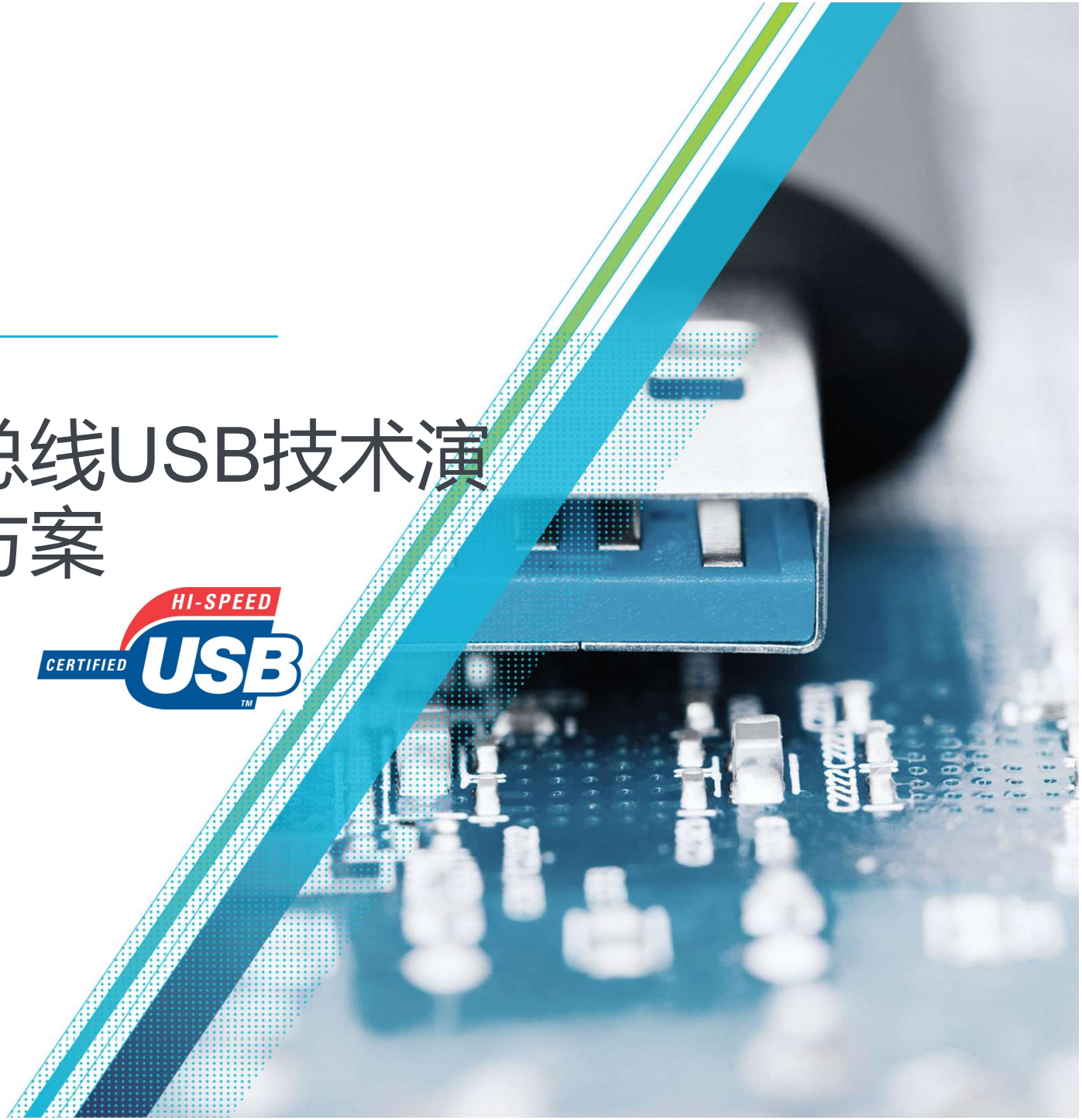
Tektronix

通用串行总线USB技术演进及测试方案

17 APRIL 2020

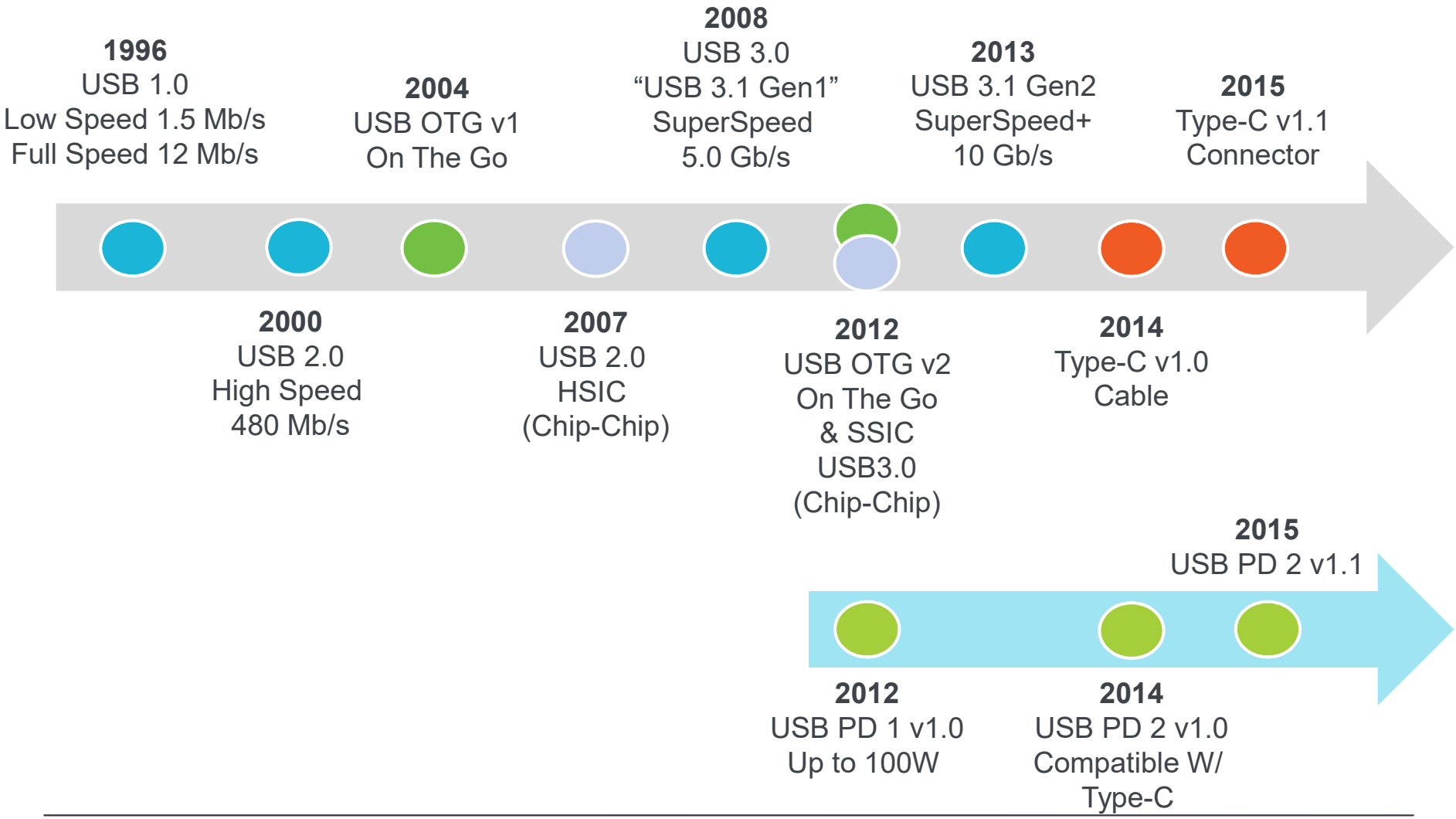


Agenda

- USB的应用场景和行业前瞻
  - 市场概况和标准发展现状
  - TypeC 接口介绍
- USB2.0一致性测试解决方案
- USB3/USB4现状及测试概况
- USB2.0测试演示

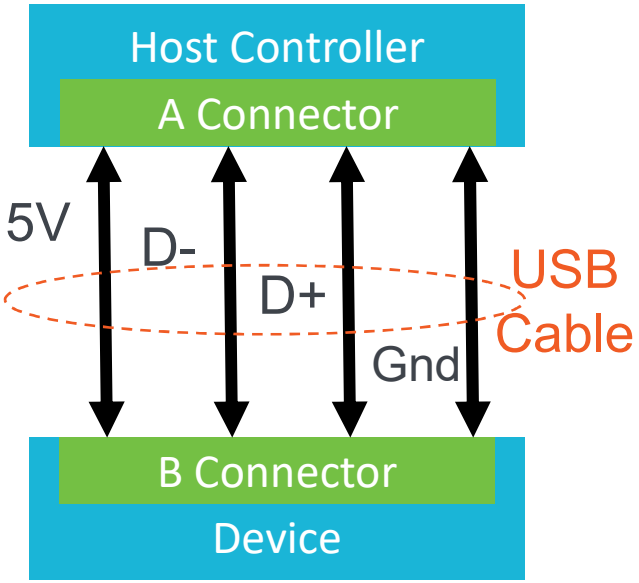
Introduction to USB

TIMELINE OF USB



Introduction to USB

FUNDAMENTALS OF USB1.X/2.0



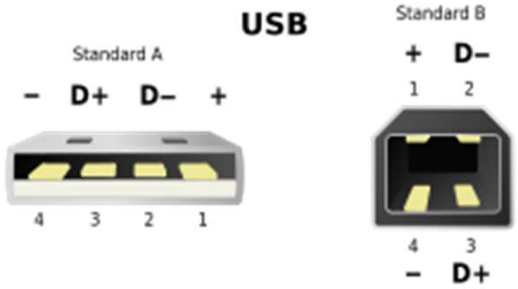
- What is USB?
  - Universal Serial Bus (USB) is a serial bus developed in 2000 with a focus of shifting from slower, wide, parallel buses to a single new high speed serial bus.
  - USB is the most successful interface in the history of the PC
  - Is made up of 4 wires (5V, Data+, Data-, Ground)
- How many variations does USB it come in?
  - USB 2.0 provides 3 speed selections, Low, Full, and High Speed. In addition are USB 3.1 Gen1/Gen2 (aka. SuperSpeed, SuperSpeed+)

Speed	Data Rate
Low Speed	1.5 Mb/s
Full Speed	12 Mb/s
High Speed	480 Mb/s
Super Speed	5 Gb/s
Super Speed+	10 Gb/s

Introduction to USB

FUNDAMENTALS OF USB1.X/2.0

- USB 2.0 supports backwards compatibility (High Speed must work with Full & Low Speed)
- Is easy to use, commonly called “hot-pluggable”
- The host uses an upstream “A” connector and devices use a downstream “B” connector.
- VBUS supplies power to devices from the host or hub. For additional power devices can have an external power supply (must be used for compliance testing)



Introduction to USB

INTEROPERABILITY CHALLENGE

Hosts

A to µB

Devices

HDDs

Flash drives

Tablets

Video Adapters

A to Std B

Hubs

A to µB

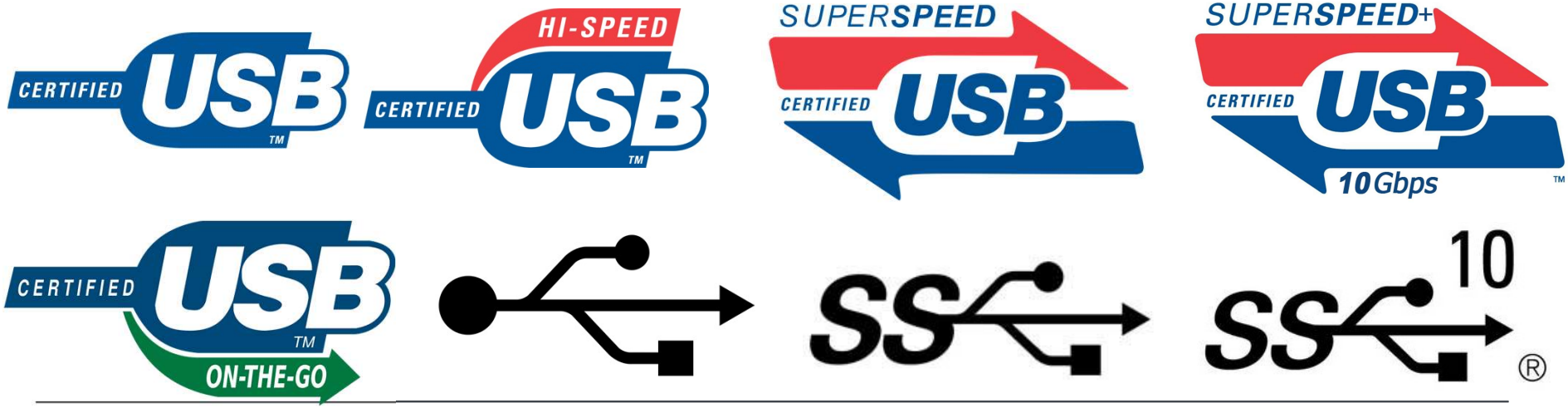
Goal: Any certified host works with any certified hub or device.

Introduction to USB

USB CERTIFICATION

Product certification and logo marking is managed by USB Implementers Forum (USB-IF) www.usb.org

- USB trademark logo indicates a device is certified and a logo license agreement has been signed. This means the device conforms to all applicable USB specifications.
- Cables / Connectors / Ports / Packaging can now be labeled with the USB logo.
- Certifies any host works with any certified hub or device.

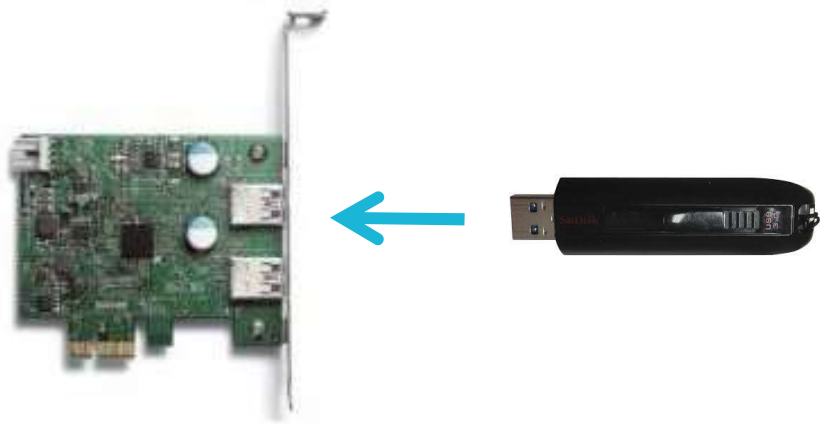


Introduction to USB

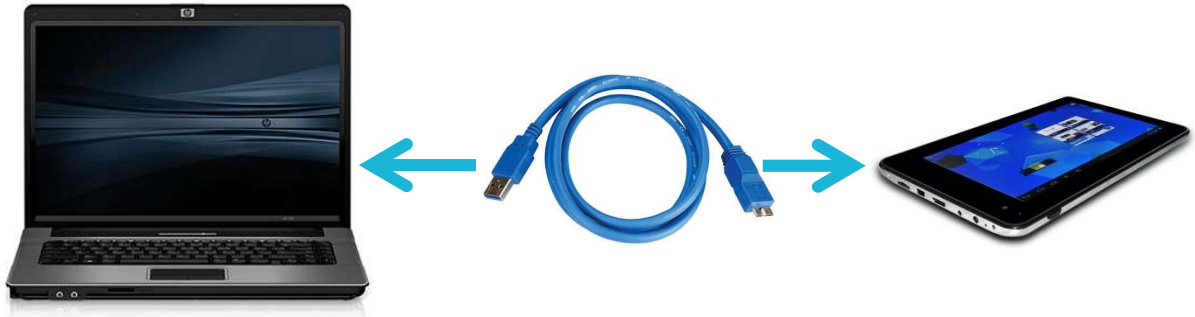
INTEROPERABILITY CHALLENGE

Goal: Any certified host works with any certified hub or device.

- Short Channel
  - 1” host PCB route
  - ¼” device PCB route
  - Direct plug



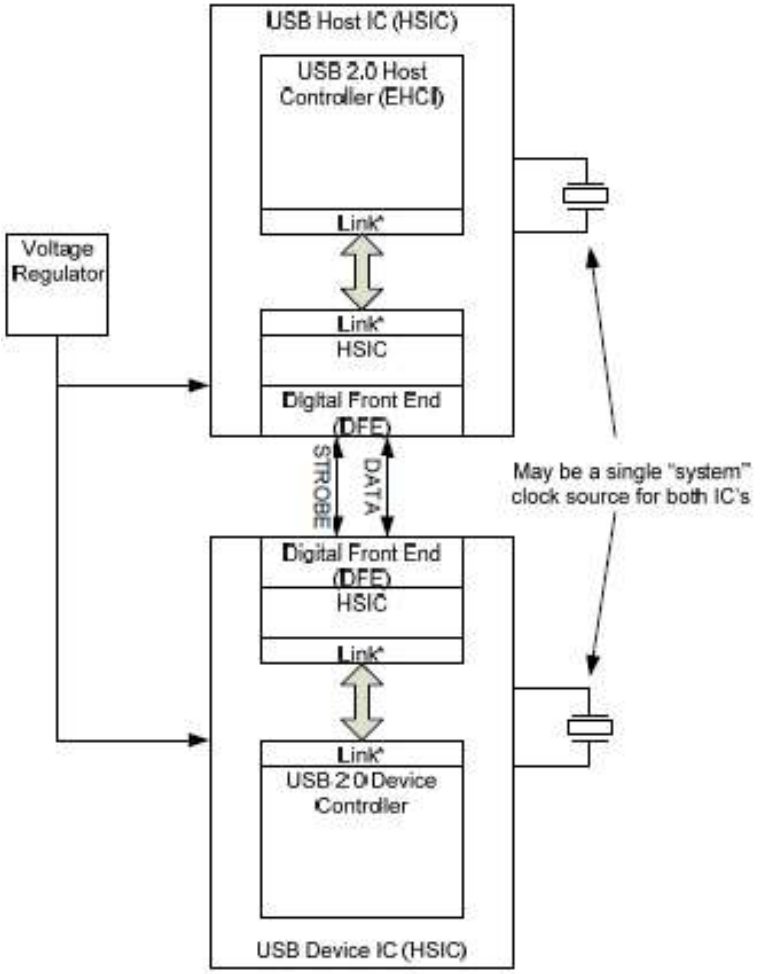
- Long Channel
  - 4” host PCB route
  - 4” device PCB route
  - 1m cable



Introduction to HSIC

HIGH SPEED INTER CONNECT (HSIC)

- What is HSIC?
  - USB 2.0 High Speed Inter Connect is a chip to chip on board serial connection.
- Why use HSIC?
  - Can replace I^2C, it's faster with no special drivers
  - Customers can reuse USB software instead of investing in multiple on board solutions
  - Super Speed Inter Connect (SSIC) brings USB 3.0 plus M-PHY together



What Does Type-C Mean to You?

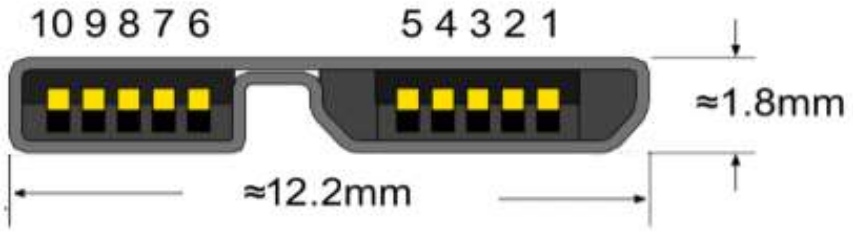
Power Delivery	More **Power** with USB Power Delivery (100 W)
Type-C	More **Flexibility** with new reversible USB Type-C connector
Alternate Mode	More **Protocols** (Display Port, Thunderbolt, HDMI, etc.)
USB IF	More **Speed** with USB 3/4

Source: USB-IF

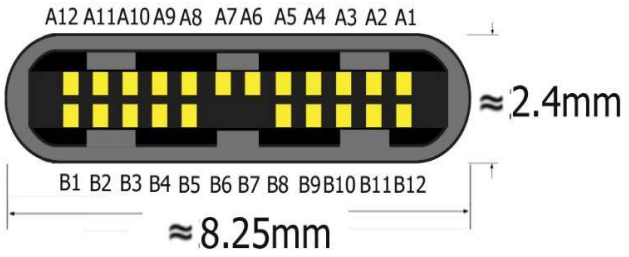
Type-C Comparison *(USB-C)*

- Rounded, reversible, flipable
- ~25% less width vs. µB
- Signaling
  - Two SS differential pairs
  - Vbus power
  - Configuration Channel (CC)
  - USB 2.0 differential pair
  - Sideband Use (SBU)
  - Plug power (Vconn)

Micro B Plug



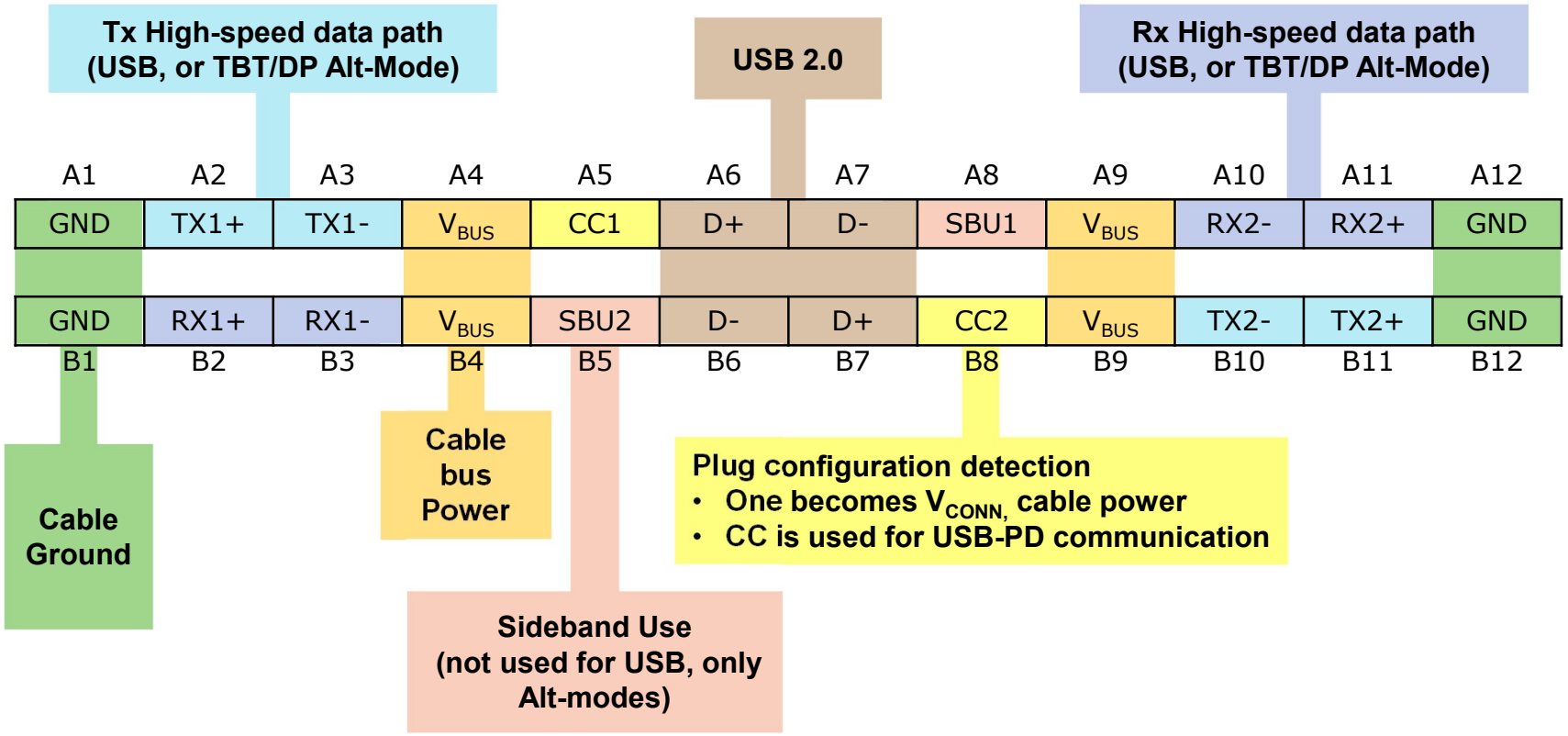
Type-C Plug



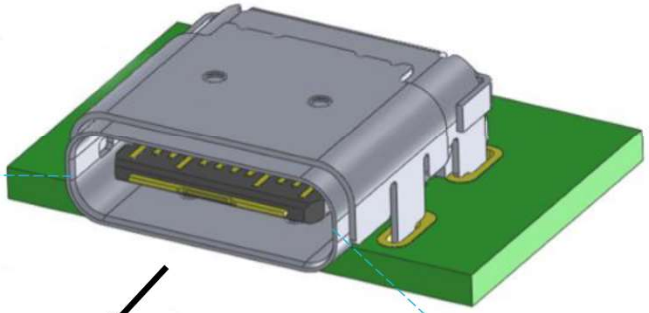
* New signals

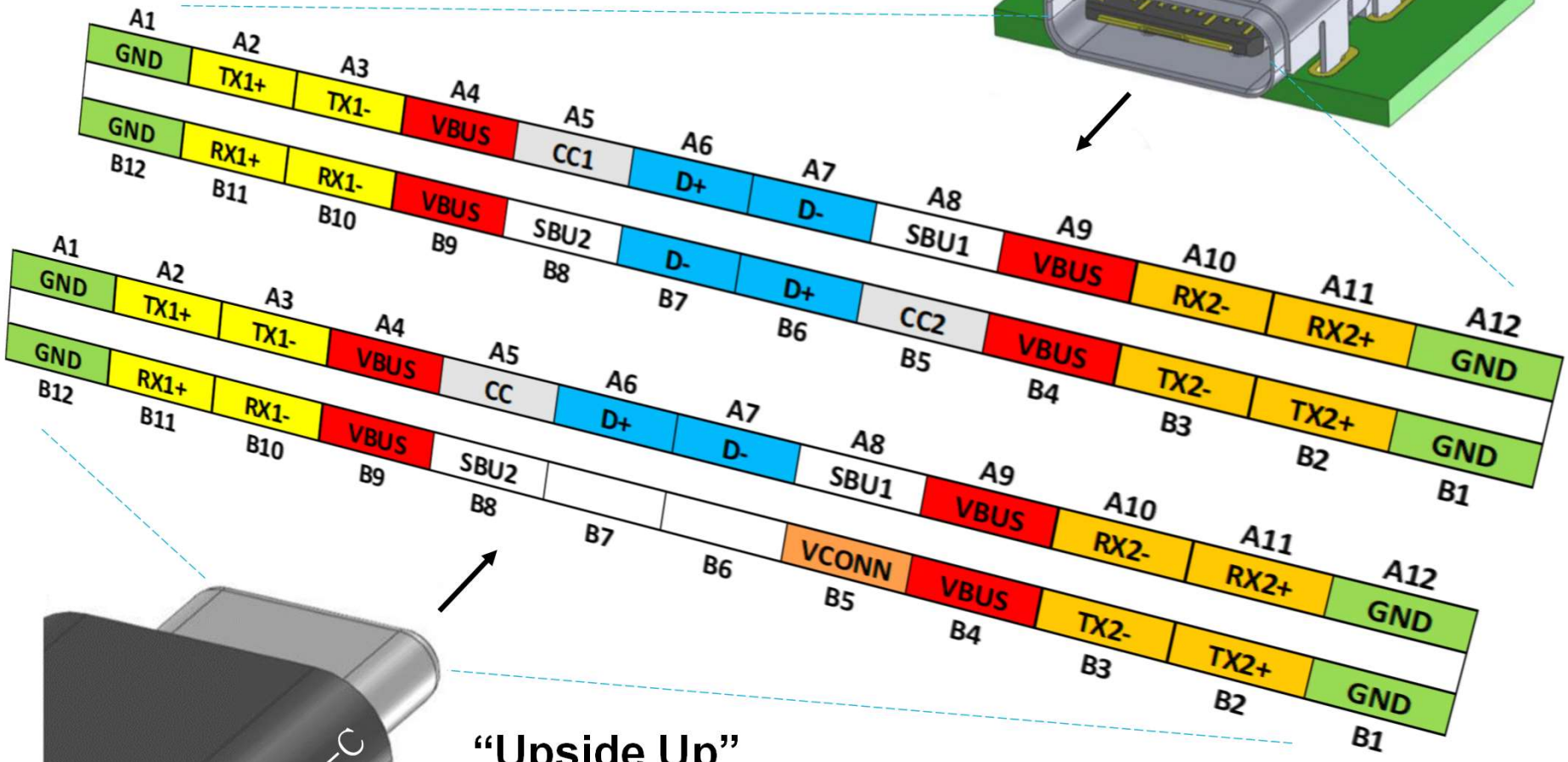
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2			VCONN	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Type-C Pin Definitions



Plug Up Orientation



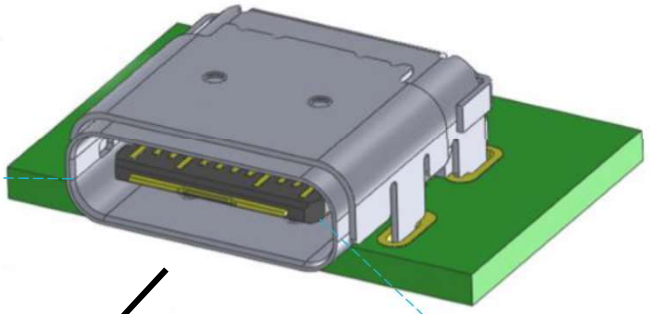


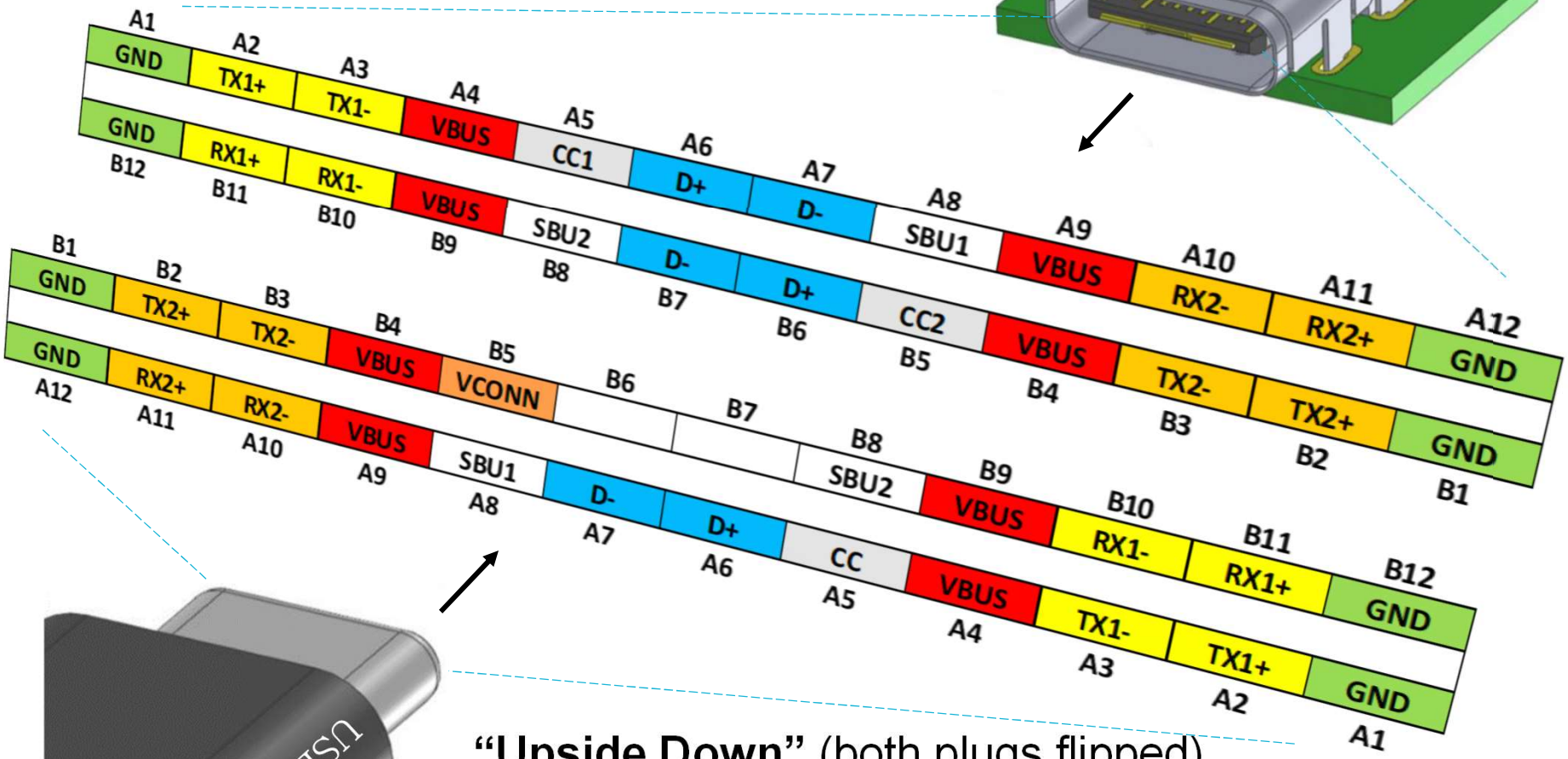
“Upside Up”

Note, end-to-end signaling have swapped pairs

(e.g. Host_A2 (TX1+) ↔ Device_A11 (RX2+))

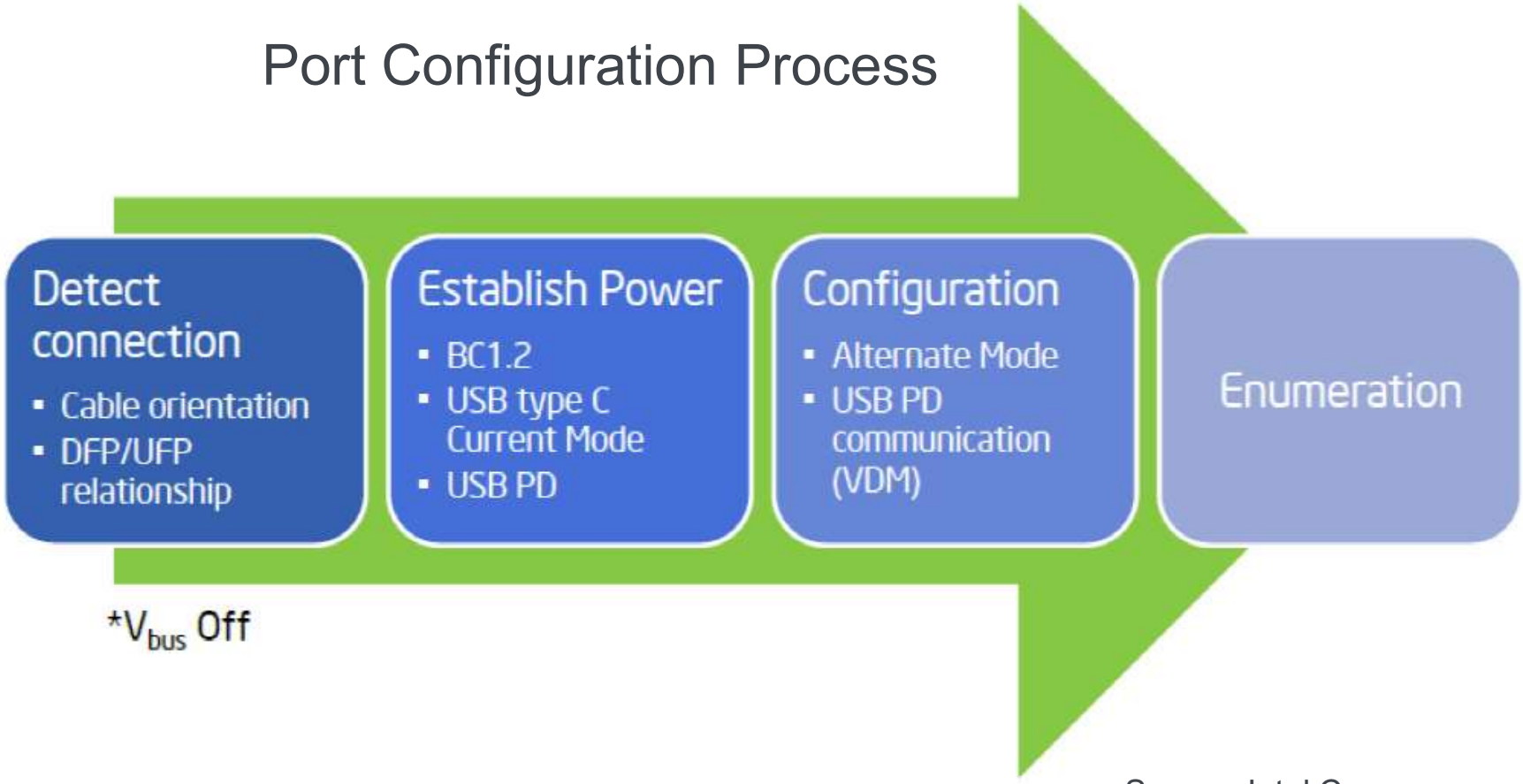
Plug Down Orientation





“Upside Down” (both plugs flipped)
Note, end-to-end signaling have swapped pairs
(e.g. Host_A2 (TX1+) ↔ Device_A11 (RX2+))

USB = Data + Video + Power



Source: Intel Corp.

Connector Transition

Legacy Cables

Plug 1	Plug 2	Version	Length
A	C	USB 2.0	≤ 4m
A	C	USB 3.1 Gen2	≤ 1m
C	B	USB 2.0	≤ 4m
C	B	USB 3.1 Gen2	≤ 1m
C	Micro-B	USB 2.0	≤ 2m
C	Micro-B	USB 3.1 Gen2	≤ 1m

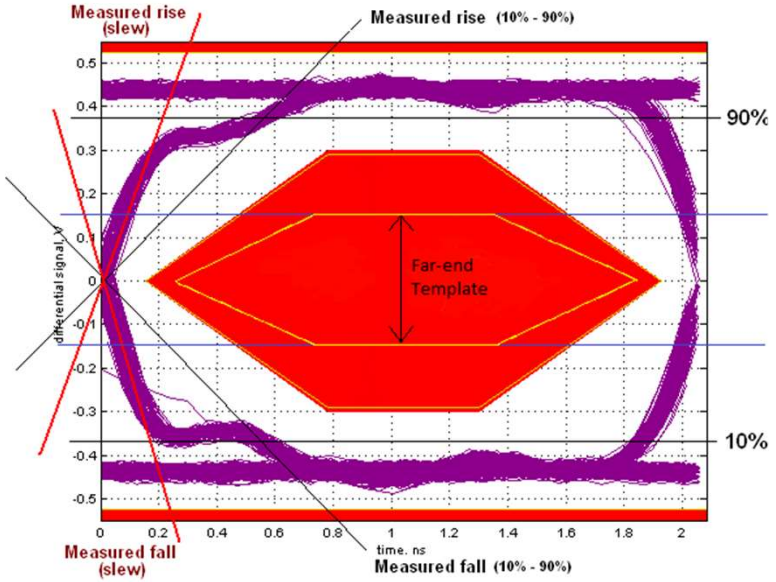
Defined Adapters

Plug 1	Plug 2	Version	Length
C	Micro-B	USB 2.0	≤ 0.15 m
C	A	USB 3.1 Gen1	≤ 0.15 m

USB 2.0 Compliance Testing

COMPLIANCE TESTING

- What is compliance testing?
  - A set of rules that define how thousands of USB hosts / hubs / device all communicate and play together nicely.
- Testing for Legacy devices (FS, LS)
  - Signal Quality, Inrush current, Drop & Droop
- High Speed specific tests
  - Signal Quality / Eye Diagram
  - Packet Parameter
  - Receiver Sensitivity
  - Timing (Suspend, Resume, Reset , Chirp)
  - Monotonicity



USB 2.0 Compliance Testing

- HOST
  - Signal Quality
  - Droop
  - Chirp
  - Suspend/Resume/Reset/Packet Parameter
- Device
  - Signal Quality
  - Suspend/Resume/Reset/Packet Parameter
  - Inrush Current
  - Chirp
  - Sensitivity
- Hub
  - Up-Stream/Down Stream

High Speed Signal Quality

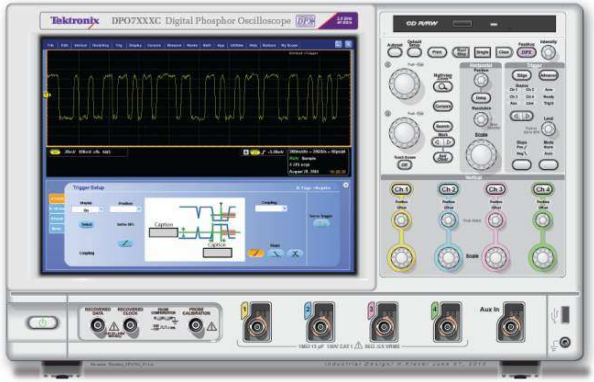
HIGH SPEED SIGNAL QUALITY TESTING INCLUDES

- What is important about Signal Quality (SQ) Testing?
  - Signal Quality Testing provides a wide assortment of base level electrical functionality testing. Allowing the user to quickly know
- What are the SQ tests?
  - Eye-Diagram testing
  - Signal Rate
  - End of Packet Width
  - Monotonicity test
  - Rise and Fall times

USB 2.0 Compliance Testing

COMPLIANCE TESTING – EQUIPMENT

- An Oscilloscope
  - MSO/DPO5000, DPO7000 or MSO/DPO70000 Series
  - 2 GHz or higher for USB 2.0 High-Speed testing
- Probes / Cables
  - 1x TDP1500, or TDP3500 differential probes
  - 3x TAP1500 single-ended probes
  - 1x TCP0030A current probe
  - 1x Matched Pair of SMA cables
- TekExpress USB2 (Option USB2) automated test software
- TDSUSBF fixture set and required USB-IF fixtures
- AWG5000C or AWG7000C signal generator for Receiver Sensitivity testing. (Receiver Sensitivity measurement is not available on the MSO/DPO5000B scopes)

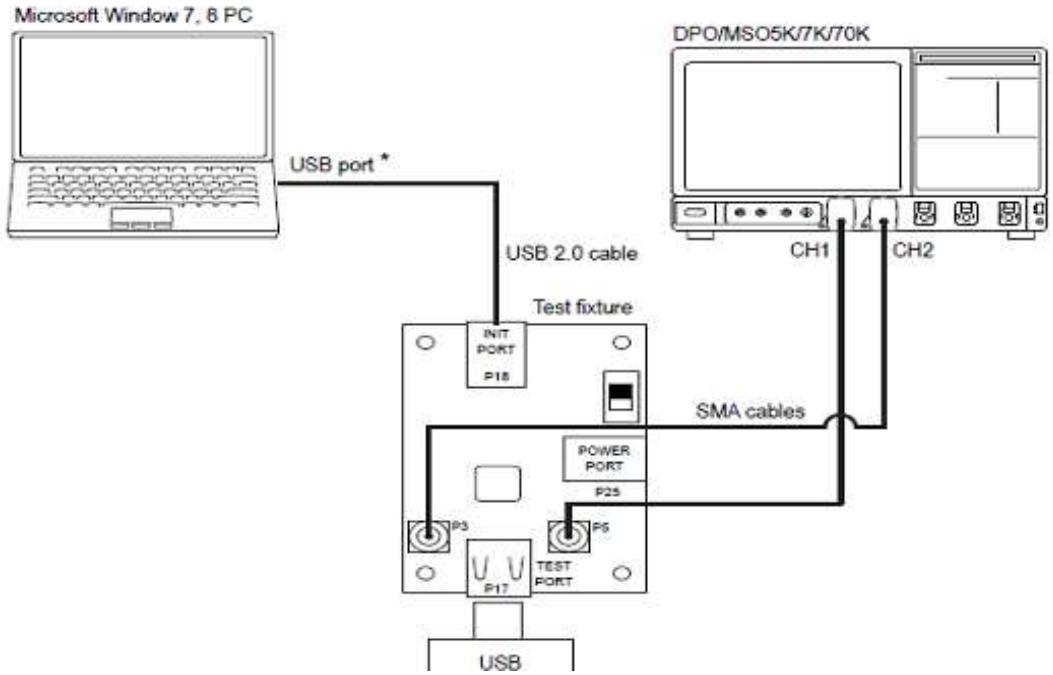


More USB test equipment details at: www.tektronix.com/USB

High Speed Signal Quality

TESTING SETUP

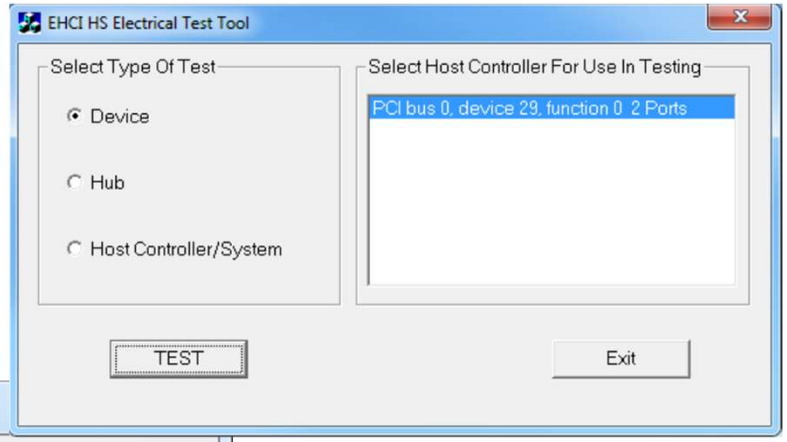
- HS Electrical Test Tool SETUP (Test_Packet)
  - A port must repetitively transmit the test packet until the exit action is taken.
  - This enables the testing of rise and fall times, eye patterns, jitter, and any other dynamic waveform specifications.

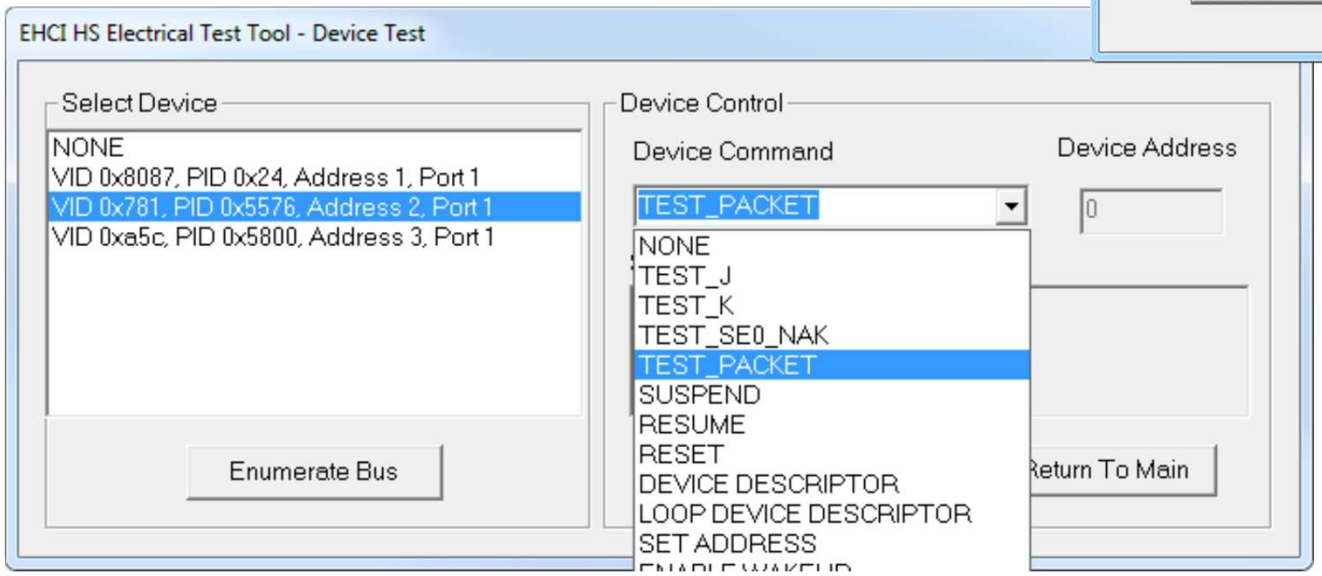


TekExpress USB2 (Opt. USB2)

HIGH SPEED ELECTRICAL TEST TOOL (HSETT)

- A USB-IF utility that enables specific test modes for official compliance testing
- Requires Win7/8/10 OS and xHCI (3.0 Host controller) or EHCI (2.0 Host controller)





High Speed Signal Quality

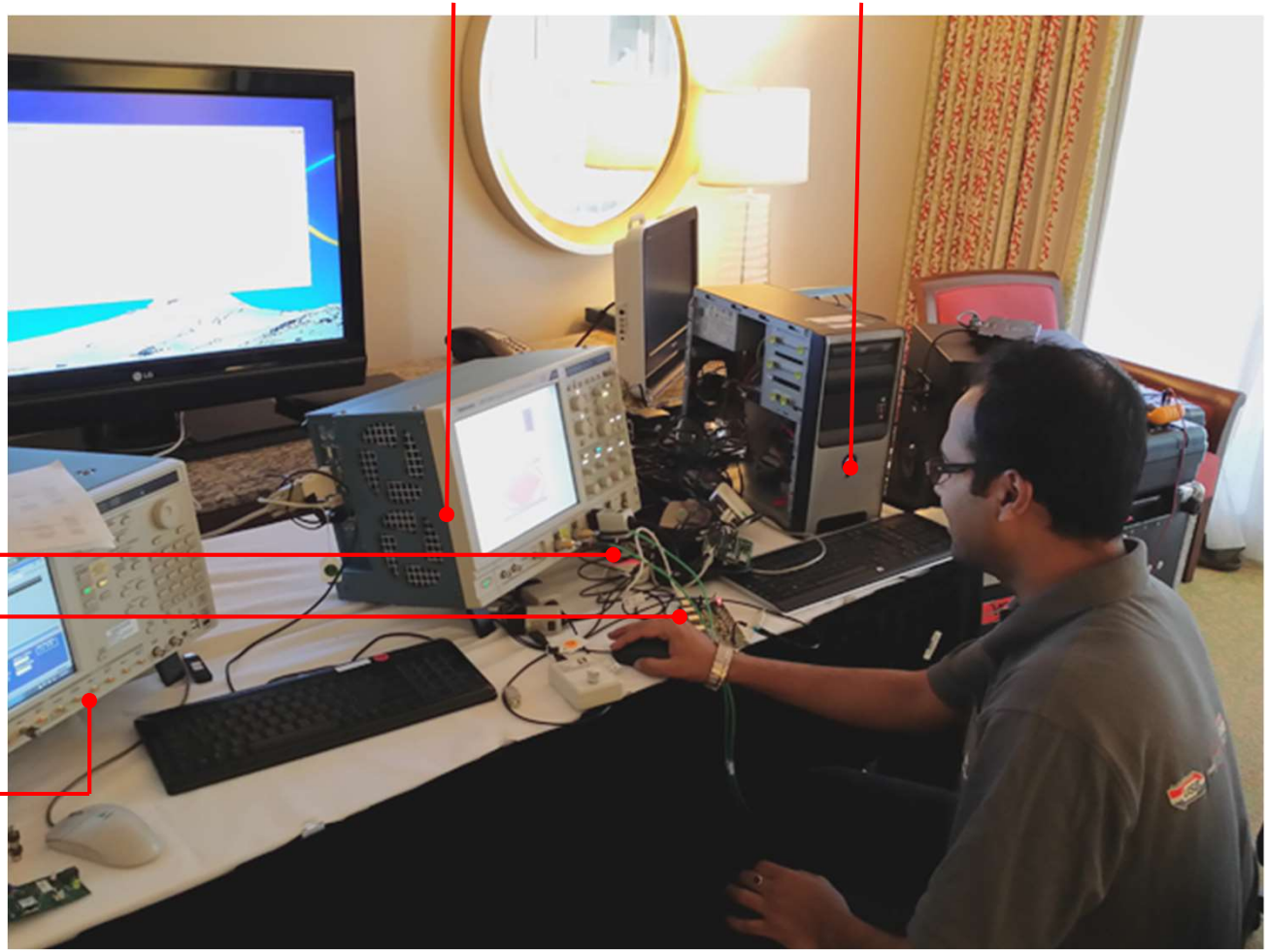
TEST PACKET FORMAT

- A port in Test_Packet mode must send this packet repetitively.

NRZI Symbols (Fields)	NRZ Bit Strings	Number of NRZ Bits
{KJ * 15}, KK (SYNC)	{00000000 * 3}, 00000001	32
KKJKJKKK (DATA0 PID)	11000011	8
JKJKJKJK * 9	00000000 * 9	72
JJKKJJKK * 8	01010101 * 8	64
JJJJKKKK * 8	01110111 * 8	64
JJJJJJKKKKKKK * 8	0, {111111S *15}, 111111	97
JJJJJJK * 8	S, 111111S, {0111111S * 7}	55
{JKKKKKKK * 10}, JK	00111111, {S0111111 * 9}, S0	72
JJJKKKJJKKKKJKKK (CRC16)	0110110101110011	16
JJJJJJJJ (EOP)	01111111	8

Compliance Testing

USB-IF 2.0 WORKSHOP



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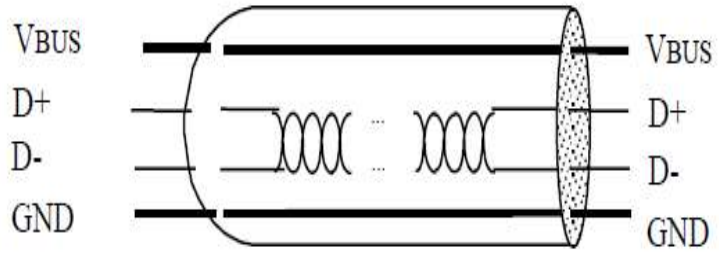
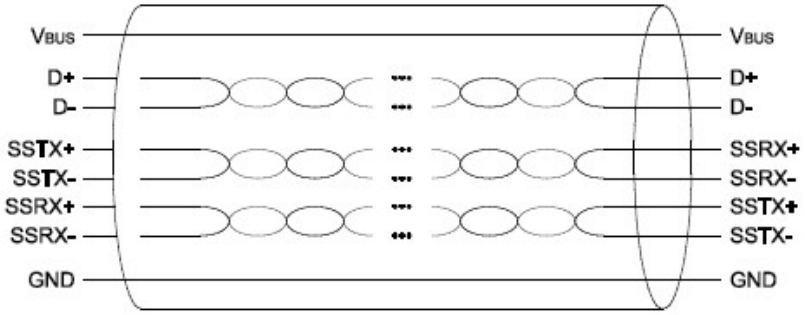
- USB2.0测试演示

Increasing Serial Data Bandwidth

- **USB 2.0, 480 Mb/s** (2000)
  - Shift from slower, wide, parallel buses to narrow, high speed serial bus
  - 40x faster data rate, support for new connectors & charging

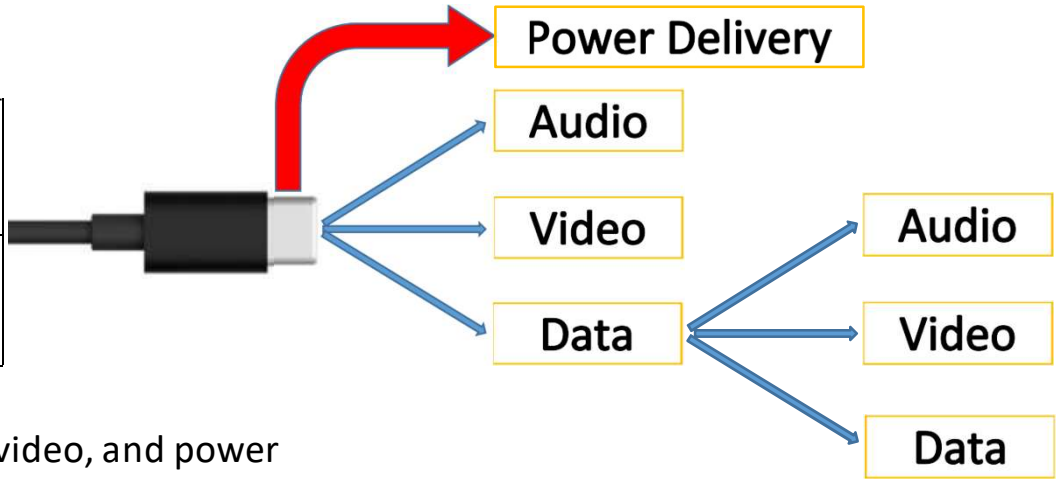


- **USB 3.0, 5 Gb/s** (2008)
  - ~10x faster data rate over 3 meter cable
  - Faster edges, ‘closed eye’ architecture



- **USB 3.1, 5/10 Gb/s** (2013)
  - 2x faster data rate over 1 meter cable
  - ‘Scaled’ SuperSpeed implementation

USB Type-C® Vision

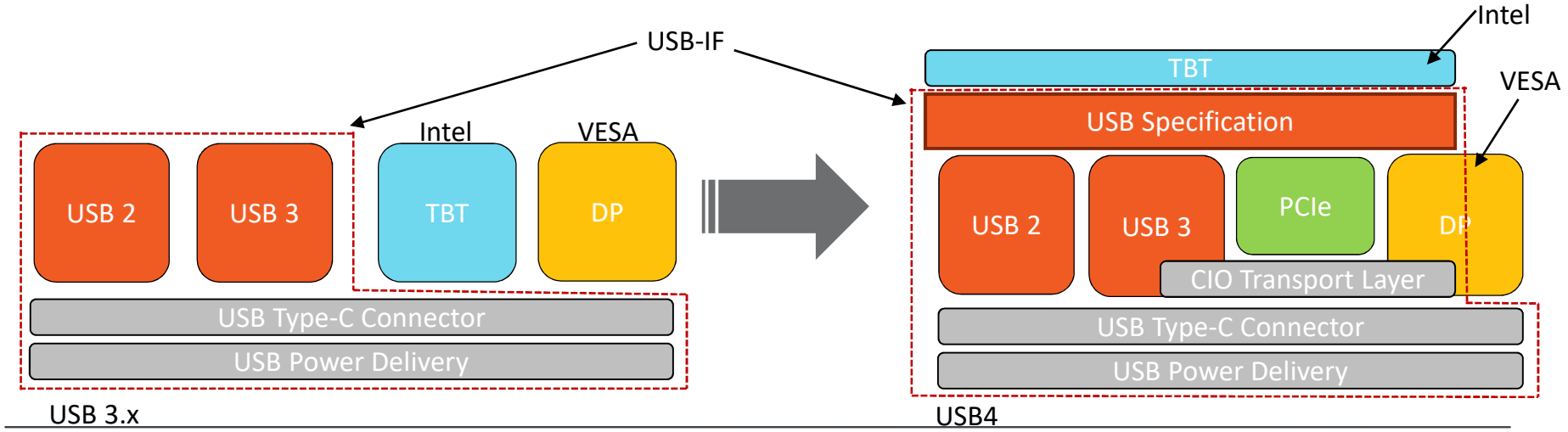


- One simple connector for data, video, and power
  - Small, flippable connector with symmetrical cables
  - Compatible systems, cables, and devices at various performance levels
- Scalable
  - Across form factors (phone to workstation), and peripherals (displays, docks, storage)
  - Across usages (low power / performance, to 8k uncompressed video)
- USB and Thunderbolt™ architecture as the foundation

USB4 Overview

MULTIPLE PROTOCOL ONTO A SINGLE PHY

- USB4 enables the next generation of USB performance over existing USB Type-C cable
  - Allows USB, DisplayPort and PCIe Tunneling (multiple protocol onto a single physical interface)
  - New signaling rates and encoding scheme
    - 10 Gbps (USB4 Gen2) works over all existing full-featured Type-C cables
    - 20 Gbps (USB4 Gen3) requires higher performance Gen3 Type-C cables
- Standards-based ownership for specification and certification
- USB4 specification is based on Thunderbolt3 specification
  - Third party vendor can build Thunderbolt3 compatible SOC or peripheral silicon

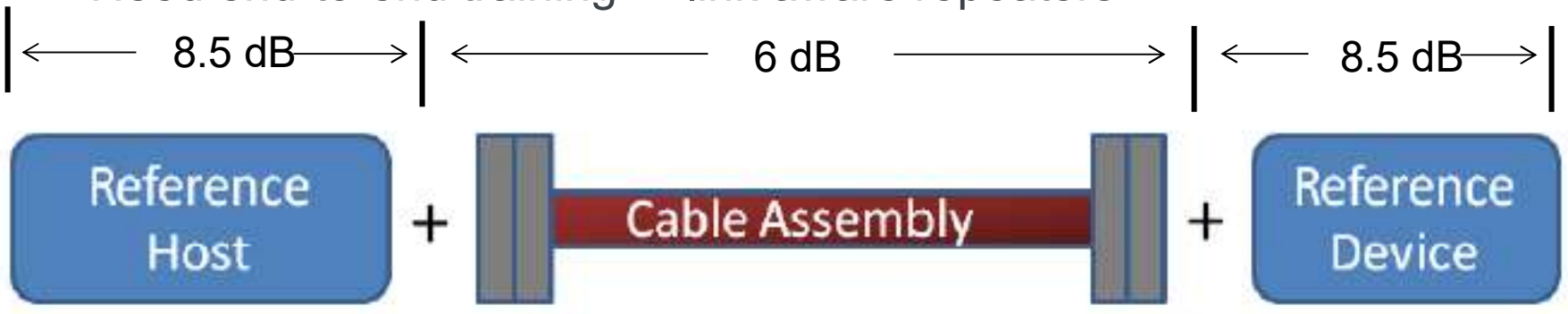


USB 3.1 Comparison

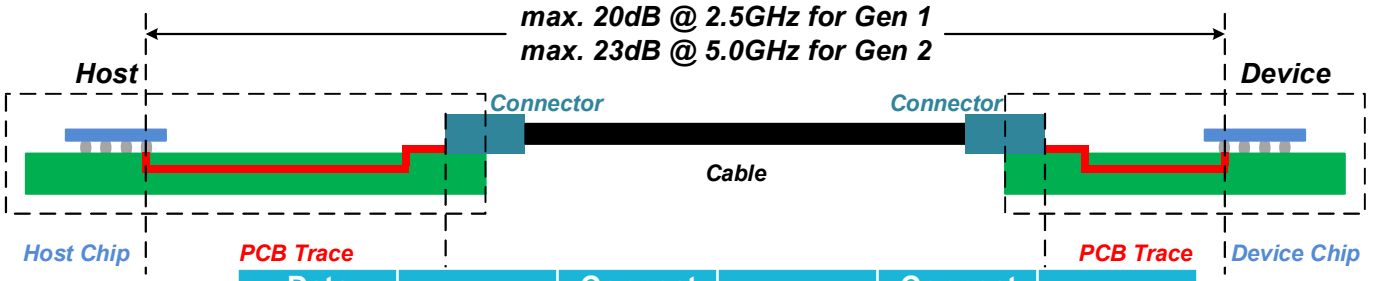
USB 3.1	Gen1	Gen2
Data Rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b
Target Channel	3m + Host/Device channels (-17dB, 2.5 GHz)	1m + board ref channels (-23dB, 5 GHz)
LTSSM	LFPS, TSEQ, TS1, TS2	LFPSPlus, SCD, TSEQ, TS1, TS2,
Reference Tx EQ	De-emphasis	3-tap (Preshoot/De-emphasis)
Reference Rx EQ	CTLE	CTLE + 1-tap DFE
JTF Bandwidth	4.9 MHz	7.5 MHz
Eye Height (TP1)	100 mV	70 mV
TJ@BER	132 ps (0.66 UI)	67.1 ps (0.671 UI)
Backwards Compatibility	Y	Y
Connector	Std. A, Micro, Type-C	Std. A, Micro, Type-C

New Channel Budget – Gen 2

- Target 23 dB @ 5 GHz loss budget (die-to-die)
- Equal channel allocation for host/device
- Tx EQ settings (normative)
  - 2.2 dB Preshoot and -3.1 dB De-emphasis
  - Requires additional compliance patterns (CP13, 14 &15) for Tx testing
- Host or device loss that exceeds 8.5 dB may required repeater
  - Need end-to-end training -> link aware repeaters



Target channel for eSS operation



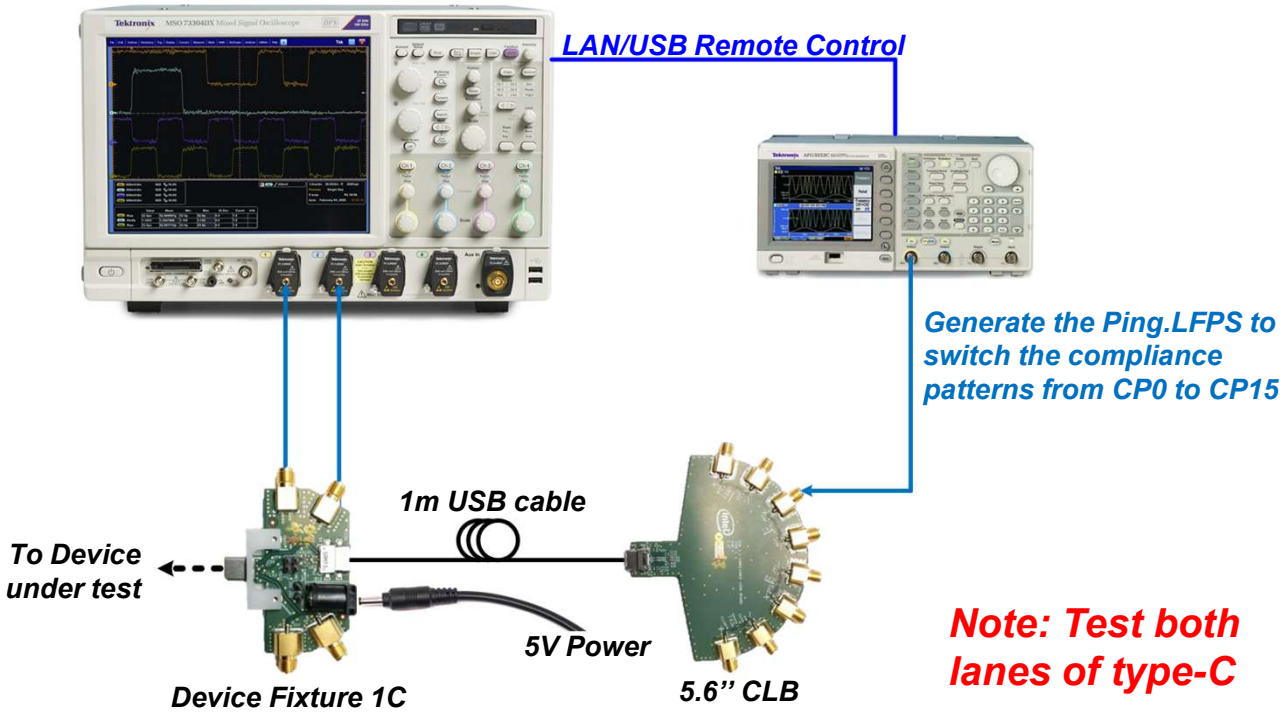
Data Rate	Host	Connector	Cable	Connector	Device
Gen 1	10dB	Std A	7.5dB	Std B	2.5dB
Gen 1	10dB	Std A	3.5dB	Micro B	6.5dB
Gen 1	10dB	Std A	3.5dB	C	6.5dB
Gen 1	6.5dB	C	7dB	Std B	2.5dB
Gen 1	6.5dB	C	4dB	Micro B	6.5dB
Gen 1	6.5dB	C	4dB	C	6.5dB
Gen 2	8.5dB	Std A	6dB	Std B	8.5dB
Gen 2	8.5dB	Std A	6dB	Micro B	8.5dB
Gen 2	8.5dB	Std A	6dB	C	8.5dB
Gen 2	8.5dB	C	6dB	Std B	8.5dB
Gen 2	8.5dB	C	6dB	Micro B	8.5dB
Gen 2	8.5dB	C	6dB	C	8.5dB

Compliance Test Item

Test ID	Test Description	
TD.1.1	Low Frequency Periodic Signaling TX Test.	LFPS Test
TD.1.2	Low Frequency Periodic Signaling RX Test.	
TD.1.3	Transmitted Eye Test at 5 GT/s	Eye Test
TD.1.4	Transmitted Eye Test at 10 GT/s	
TD.1.5	Transmit Equalization Test at 10 GT/s	TX EQ Test
TD.1.6	Transmitted SSC Profile Test at 5 GT/s	SSC Test
TD.1.7	Transmitted SSC Profile Test at 10 GT/s	
TD.1.8	Receiver Jitter Tolerance Test at 5 GT/s	RX JT Test
TD.1.9	Receiver Jitter Tolerance Test at 5 GT/s (Type-C)	
TD.1.10	Receiver Jitter Tolerance Test at 10 GT/s	

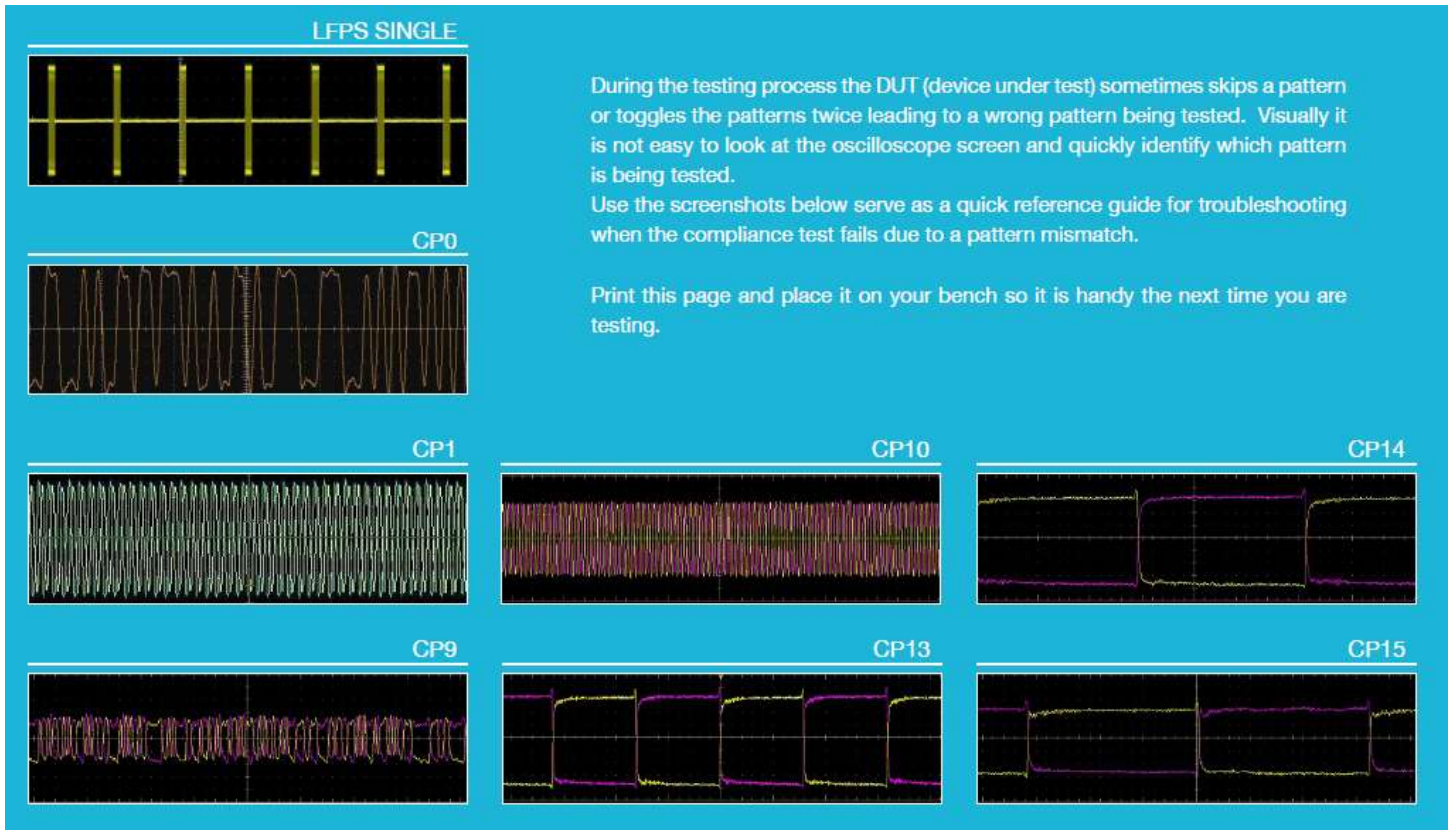
Tx Compliance Test

Example of Test Setup: Type-C Device

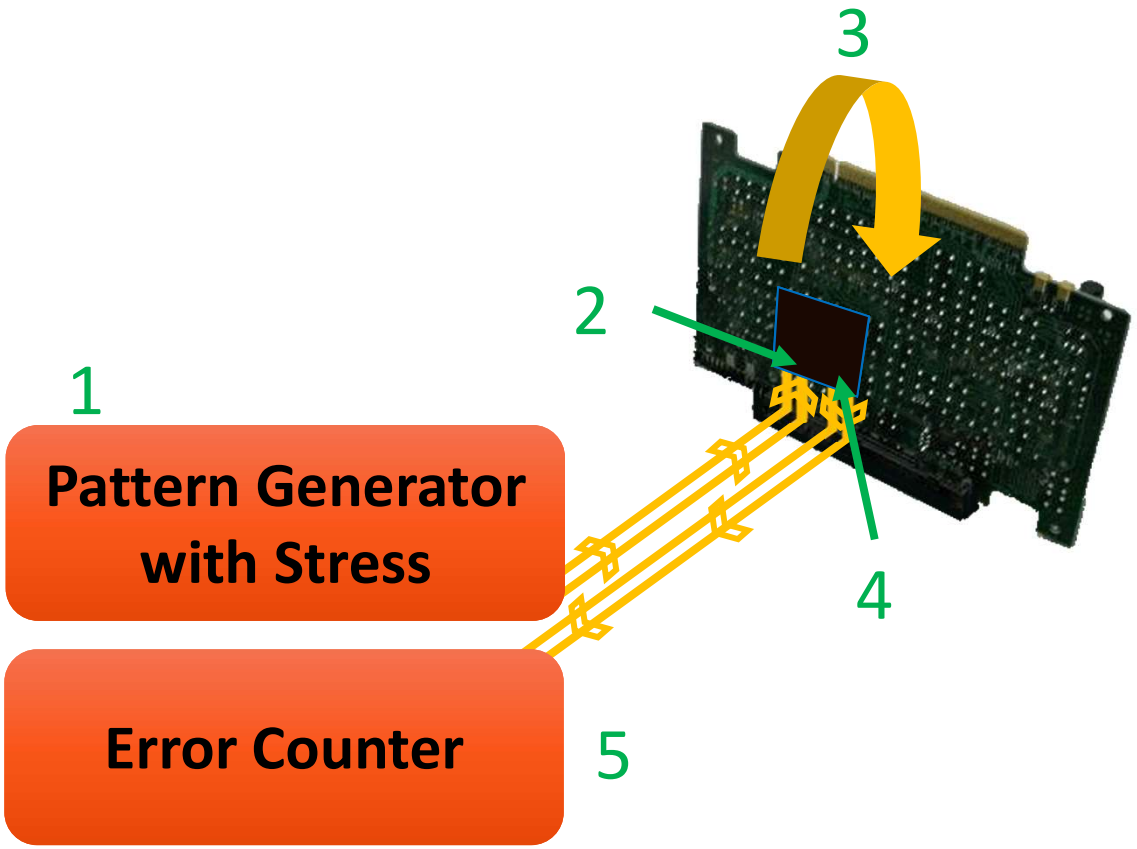


Note: Test both lanes of type-C

Compliance Test Pattern



Basics of Rx Testing

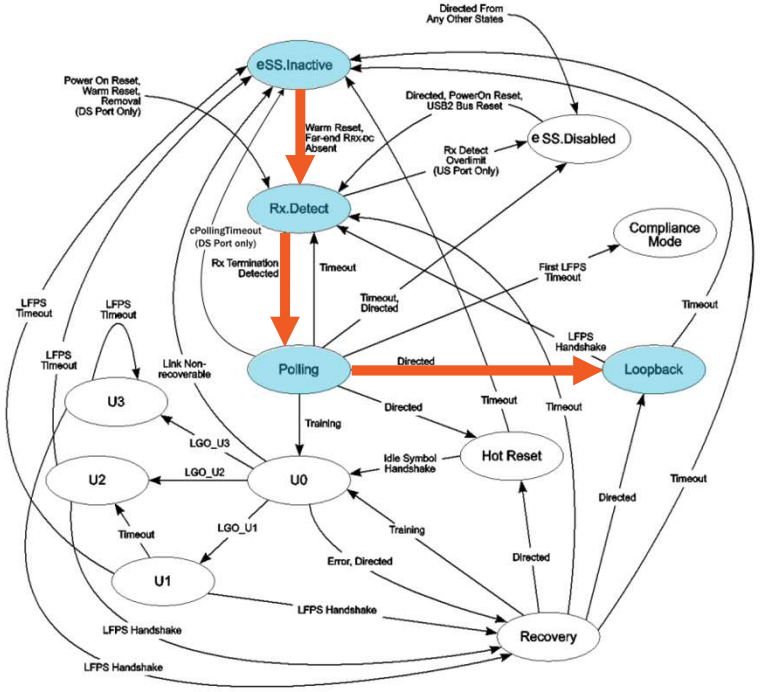


At the simplest level, receiver testing is composed of:

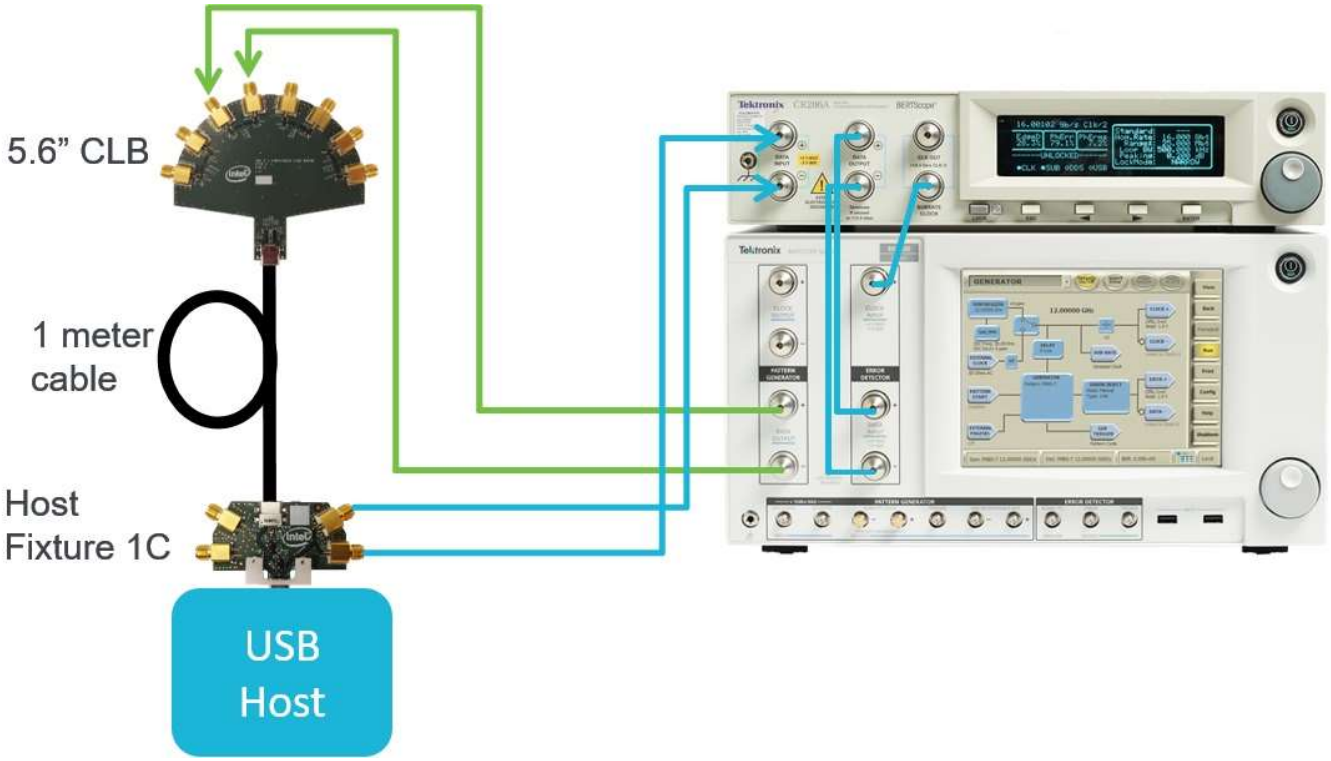
1. Send impaired signal to the receiver under test
2. The receiver decides whether the incoming bits are a one or a zero
3. The chip loops back the bit stream to the transmitter
4. The transmitter sends out exactly the bits it received
5. An error counter compares the bits to the expected signal and looks for mistakes (errors)

Getting a DUT Into Loopback Mode

- Basic Overview
  - DUT starts in Power-off, or test fixture un-plugged
  - At device power-on or hot plug, BERT sends LFPS signaling
  - Device responds by going from LFPS.Polling to training sequence
    - Handshaking sequence between DUT and BERT: TSEQ > TS1 > TS2
    - TS2 sequence from BERT sets loopback bit to force DUT into loopback for Rx testing

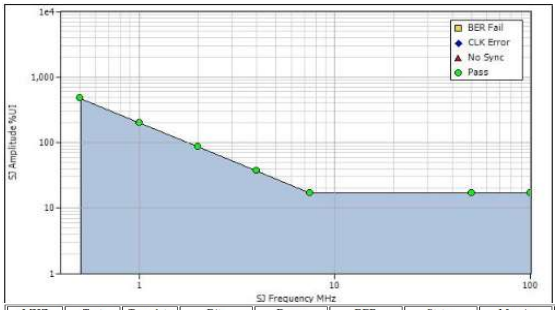


BERTScope (BSX) USB 3.1 RX Test Configuration



Receiver Tolerance Test Overview

- Nine Test Points (USB3.1 Gen2)
- SSC Clocking is enabled
- Preshoot/De-emphasis enabled
- Stress verified by TJ/Eye Height
- Each SJ term in the table is tested one at a time after the device is in loopback mode



MHZ	Test	Template	Bits	Errors	BER	Status	Margin
0.50	476.00%	476.00%	3.00e010	0	0.00e000	Passed	0.00%
1.00	203.00%	203.00%	3.00e010	0	0.00e000	Passed	0.00%
2.00	87.00%	87.00%	3.00e010	0	0.00e000	Passed	0.00%
4.00	37.00%	37.00%	3.00e010	0	0.00e000	Passed	0.00%
7.50	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
50.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
100.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%

Frequency	SJ	RJ
500kHz	476ps	1.308ps RMS
1MHz	203ps	1.308ps RMS
2MHz	87ps	1.308ps RMS
4MHz	37ps	1.308ps RMS
7.5MHz	17ps	1.308ps RMS
15MHz	17ps	1.308ps RMS
30MHz	17ps	1.308ps RMS
50MHz	17ps	1.308ps RMS
100MHz	17ps	1.308ps RMS

Agenda

- USB的应用场景和行业前瞻
  - 市场概况和标准发展现状
  - TypeC 接口介绍
- USB2.0一致性测试解决方案
- USB3/USB4现状及测试概况
- USB2.0测试演示

答疑环节