直播大讲堂—DDR的原理及信号完整性测试

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2020/5/22

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主题	时间
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PCIe GEN5 PHY 规范更新解读与测试揭秘	4.10
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MIPI/LVDS物理层测试解决方案	5.15
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三相逆变器电机驱动原理分析与测试应用	6.5

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	日程
14：30 - 15：30	**DDR的技术发展和演变路线** • 标准发展现状 • 基本架构 **DDR3测试所面临的困难与挑战** • 信号探测/读写分离的困难 **泰克DDR3一致性解决方案** • 信号探测方案——BGA Interposer • 可视触发功能 • TekExpress DDR一致性方案
15：30 - 15：45	**答疑**
15：45 - 16：00	**抢答有奖**

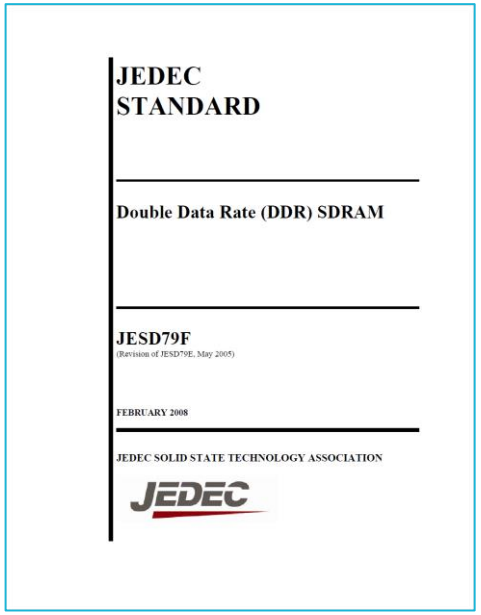
Tektronix

DDR原理及信号完整性测试

DDR的演变和基本原理

DDR的相关标准概览

JEDEC组织开发的DDR标准，从DDR1到DDR5


JEDEC
STANDARD

Double Data Rate (DDR) SDRAM

JESD79F
(Revision of JESD79E, May 2005)

FEBRUARY 2008

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

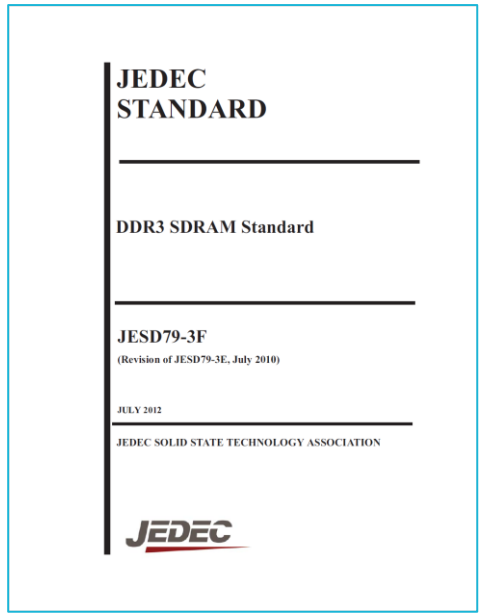

JEDEC
STANDARD

DDR2 SDRAM SPECIFICATION

JESD79-2F
(Revision of JESD79-2E)

November 2009

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

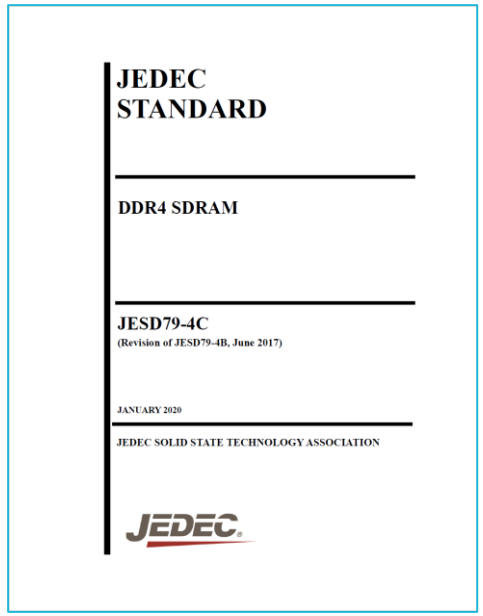

JEDEC
STANDARD

DDR3 SDRAM Standard

JESD79-3F
(Revision of JESD79-3E, July 2010)

JULY 2012

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION


JEDEC
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DDR4 SDRAM

JESD79-4C
(Revision of JESD79-4B, June 2017)

JANUARY 2020

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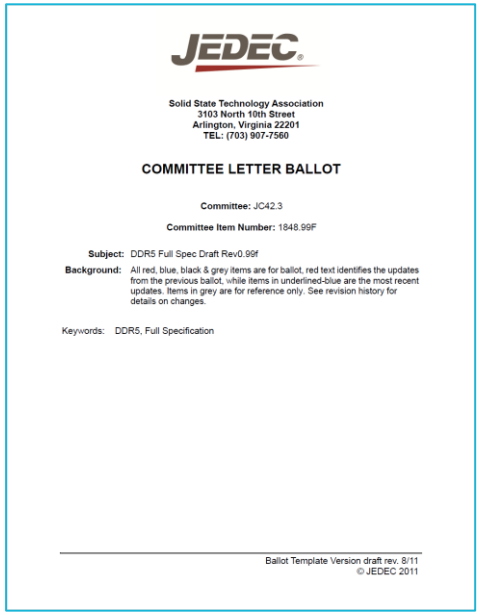
Solid State Technology Association
3103 North 10th Street
Arlington, Virginia 22201
TEL: (703) 907-7560

COMMITTEE LETTER BALLOT

Committee: JC42.3

Committee Item Number: 1848.99F

Subject: DDR5 Full Spec Draft Rev0.99f

Background: All red, blue, black & grey items are for ballot, red text identifies the updates from the previous ballot, while items in underlined-blue are the most recent updates. Items in grey are for reference only. See revision history for details on changes.

Keywords: DDR5, Full Specification

Ballot Template Version draft rev. 8/11
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- JEDEC，全称为“Joint Electron Device Engineering Council”，固态技术协会，为一个全球性的组织
- 所有的DDR标准、LPDDR标准、GDDR标准，及内存模组标准均是由JEDEC下属的 JC-42 Solid State Memories工作组所开发。

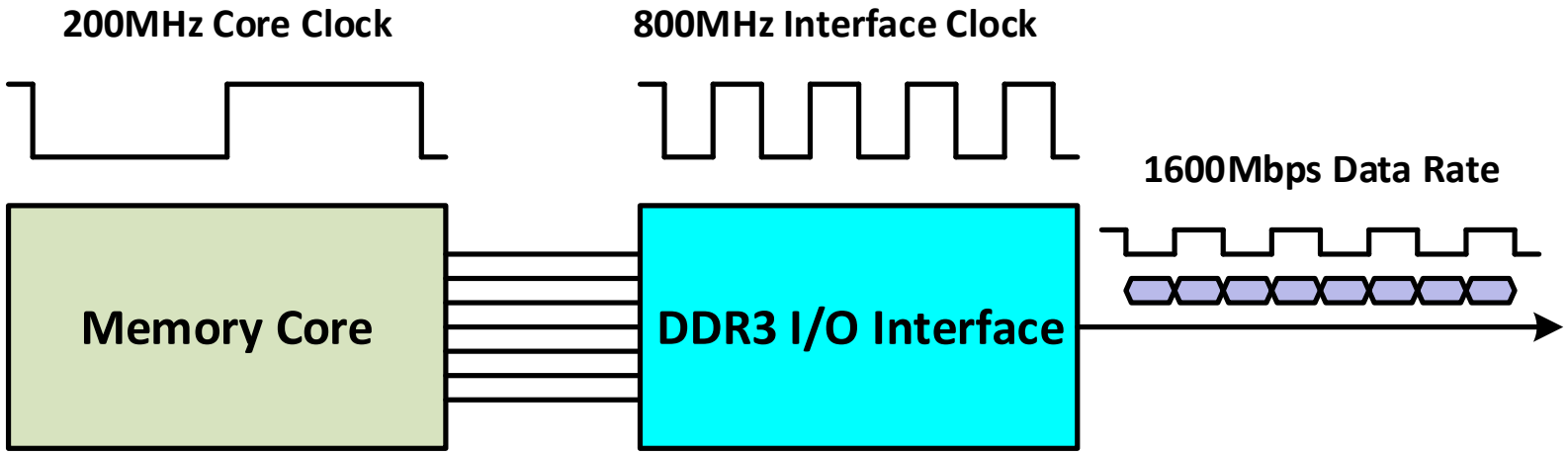
从DDR1到DDR5的演变

电压更低，速率翻倍，容量翻倍

Gens	Release Year	Voltage	Data Rate	Density	Number of Banks	Prefetch Architecture	Supported Burst Length
DDR1	2000	2.5/2.6 V	200 MT/s ~ 400 MT/s	64 Mb ~ 1 Gb	4	2n-prefetch	2, 4, 8
DDR2	2003	1.8 V	400 MT/s ~ 800 MT/s	256 Mb ~ 4 Gb	4, 8	4n-prefetch	4, 8
DDR3	2007	1.5/1.35 V	800 MT/s ~ 2133 MT/s	512 Mb ~ 8 Gb	8	8n-prefetch	BC4, BL8
DDR4	2014	1.2 V	1600 MT/s ~ 3200 MT/s	2 Gb ~ 16 Gb	8, 16	8n-prefetch + bank grouping	BC4, BL8
DDR5	2020	1.1 V	3200 MT/s ~ 6400 MT/s	8 Gb ~ 32 Gb	8, 16, 32	16n-prefetch + bank grouping	BC8, BL16, BL32

下一代在上一代基础上，速率翻倍，容量翻倍

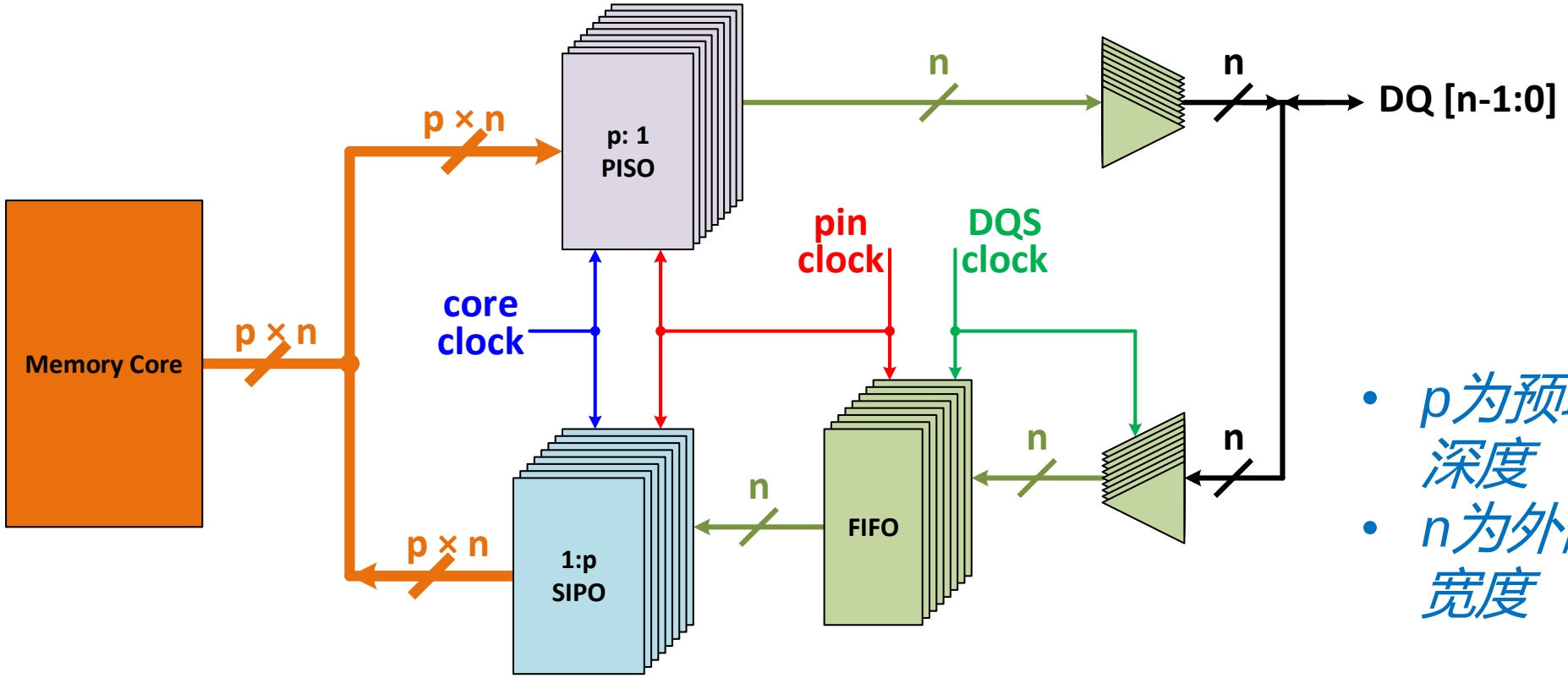
DDR接口的基本原理



- 内核的频率：100MHz~266MHz，从SDR时代到DDR，再到最新的DDR5；
- 数据速率的提升是通过I/O接口的架构设计实现的，主要有三个技术：
  - ✓ 双边沿传输数据：这是DDR名称的来源；
  - ✓ 预取技术(Prefetch): 2bit for DDR, 4bit for DDR2, 8bit for DDR3, 8bit for DDR4, 16bit for DDR5…本质上是一个串并转换技术；
  - ✓ SSTL/POD Signaling: 克服在高速传输时的信号完整性的问题

DDR接口的基本原理

芯片内部的一般架构：保证数据能够高速从芯片引脚输出



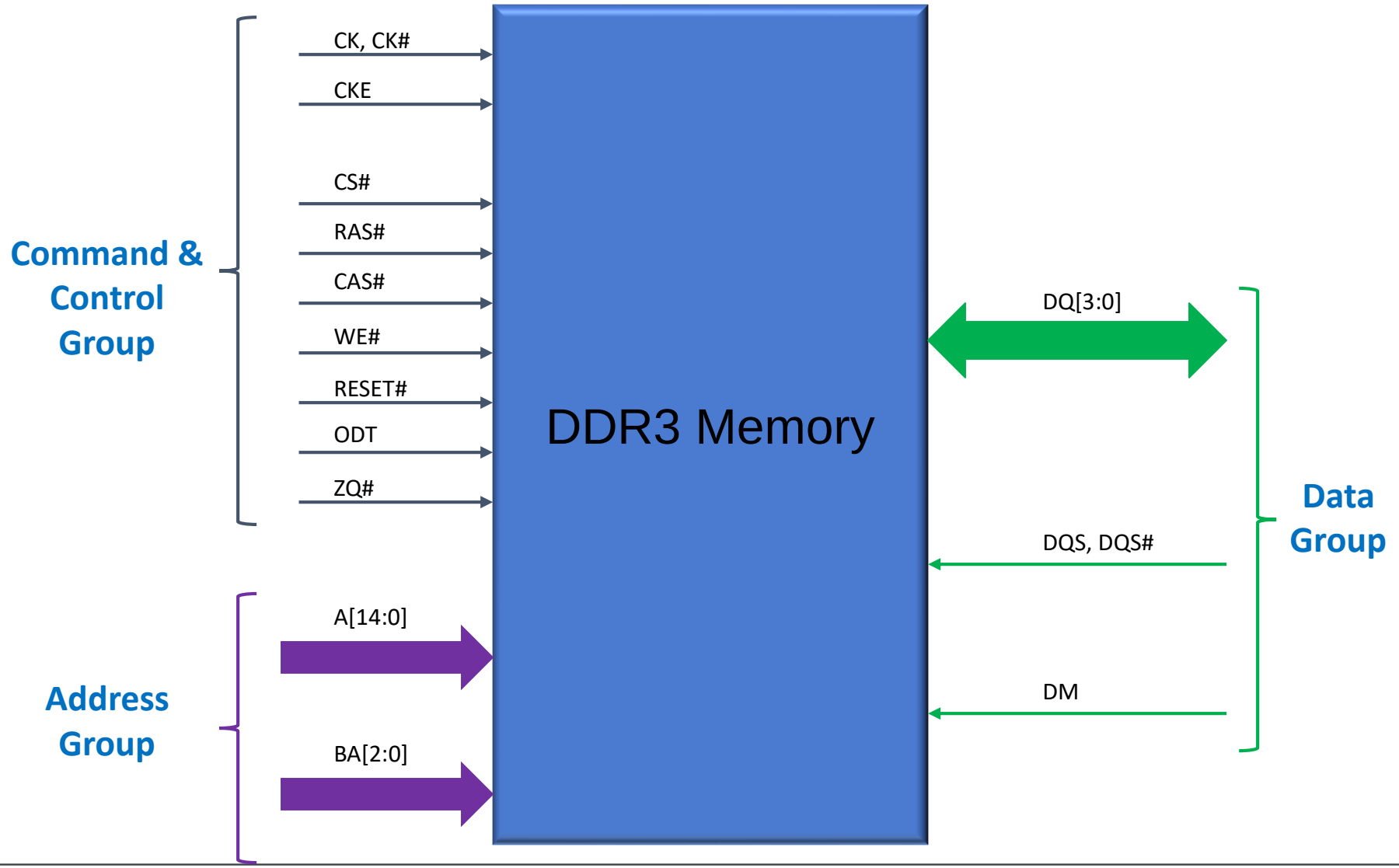
- *p为预取（prefetch）深度*
- *n为外部DQ总线的宽度*

在上述这样一种芯片架构中，为了最大程度的降低DRAM芯片的成本，最省成本的方法为：

- 对于读操作，DQS与DQ为边沿对齐；
- 对于写操作，DQS与DQ为中心对齐；

对DDR接口信号进行分类

引脚框图



对DDR接口信号进行分类

信号分类及其拓扑连接方式

Group	x4	x8	x16
Data Group	DQ[3:0]	DQ[7:0]	DQU[7:0], DQL[7:0]
	DQS, DQS#	DQS, DQS#	DQSU, DQU#
			DQSL, DQL#
	DM	DM	DMU
			DML
	/	TDQS, TDQS#	/
Address Group	A[14:13]	A[14:13]	A[14:13]
	A12/BC#	A12/BC#	A12/BC#
	A11	A11	A11
	A10/AP	A10/AP	A10/AP
	A[9:0]	A[9:0]	A[9:0]
	BA[2:0]	BA[2:0]	BA[2:0]
Command Group	RAS#	RAS#	RAS#
	CAS#	CAS#	CAS#
	WE#	WE#	WE#
Control Group	RESET#	RESET#	RESET#
	CS#	CS#	CS#
	CKE	CKE	CKE
	ODT	ODT	ODT
Clock Group	CK, CK#	CK, CK#	CK, CK#

point-to-point topology for the same rank; parallel for different ranks

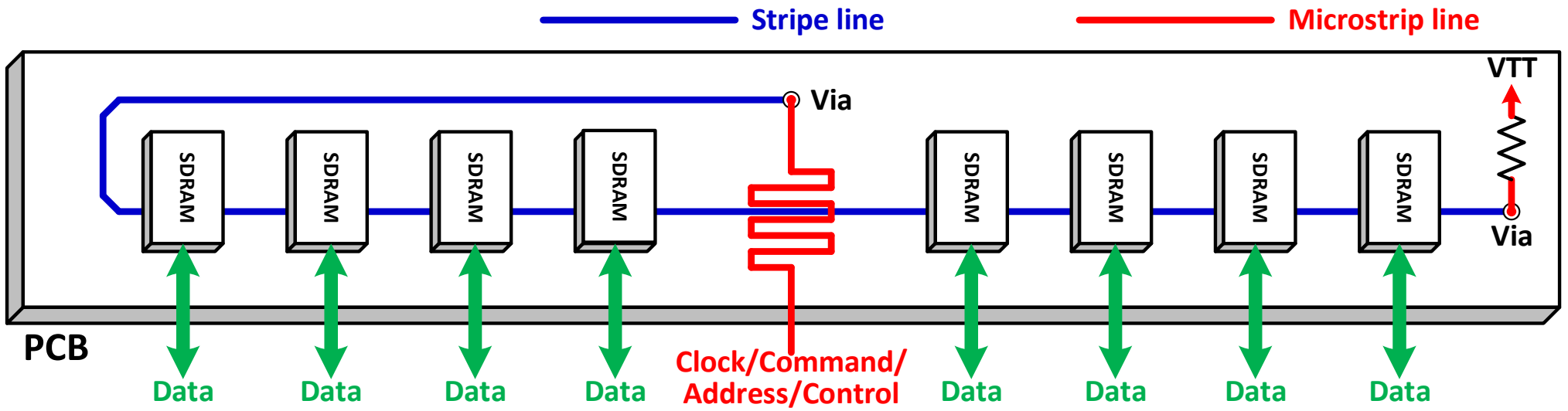
fly-by topology for layout

point-to-point topology for the same rank; independent for different ranks

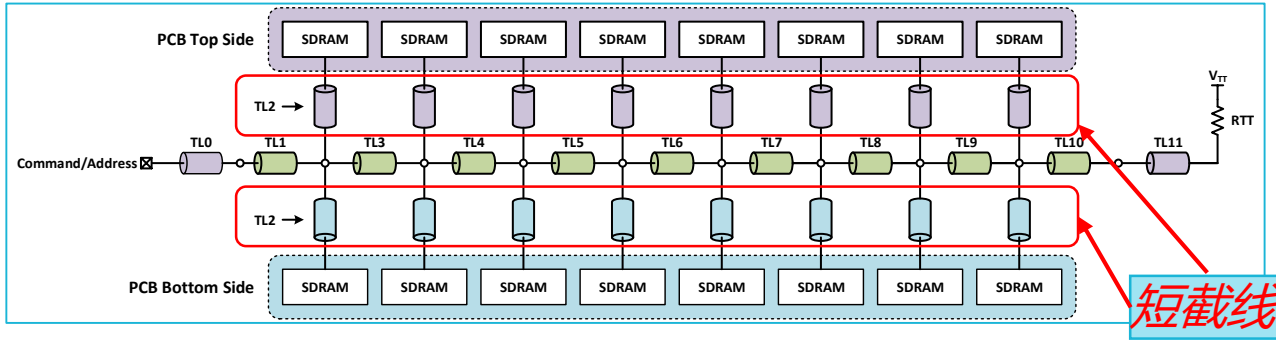
fly-by topology for layout

不同类的信号，它的拓扑连接方式不一样

Layout of DDR3 DIMM as an Example

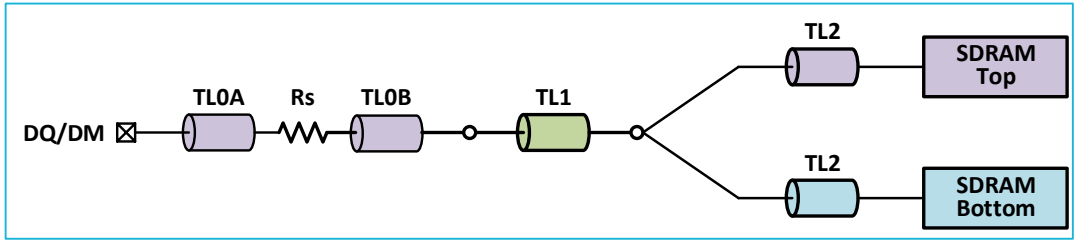


fly-by型的菊花链拓扑: 克服多负载的信号完整性问题

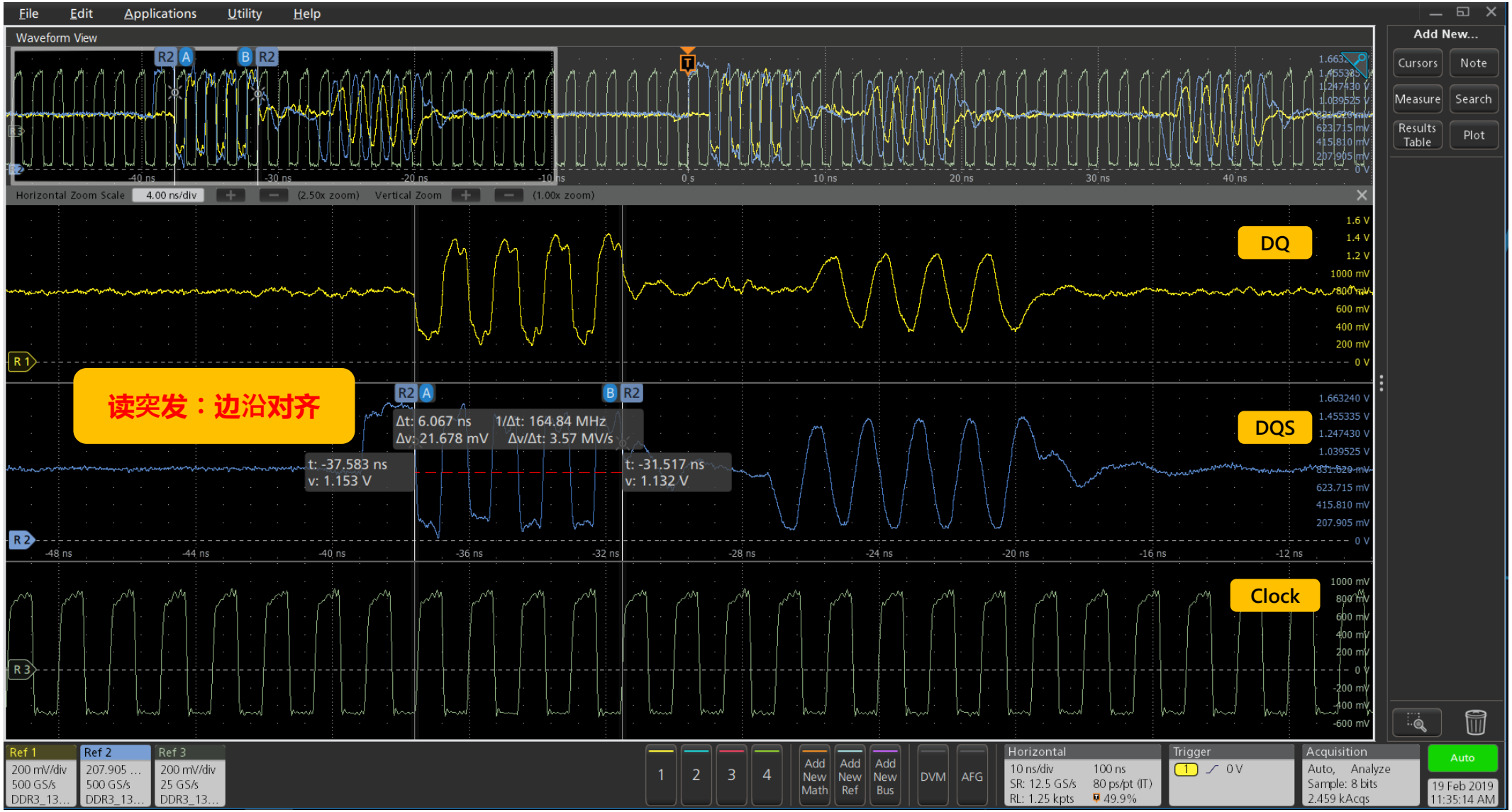


短截线TL2尽可能地短

Pt2P拓扑



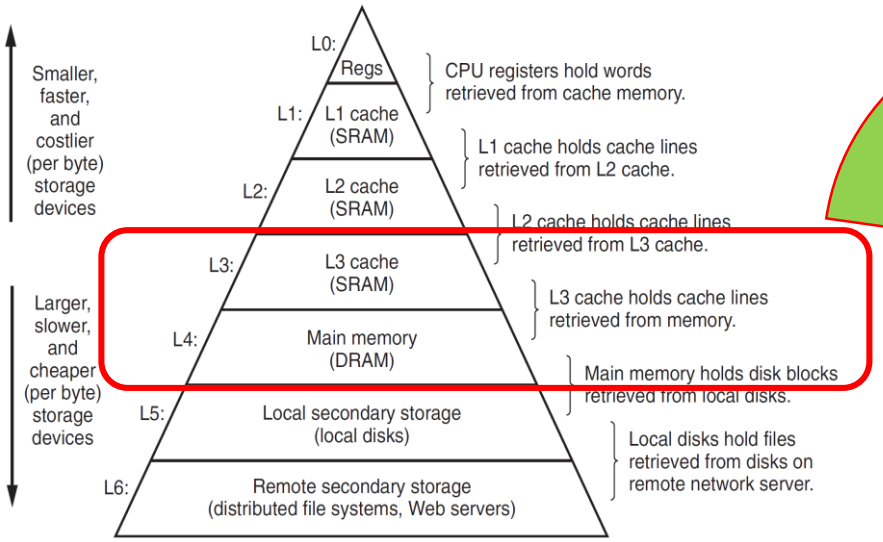
DDR3 Read and Write Burst

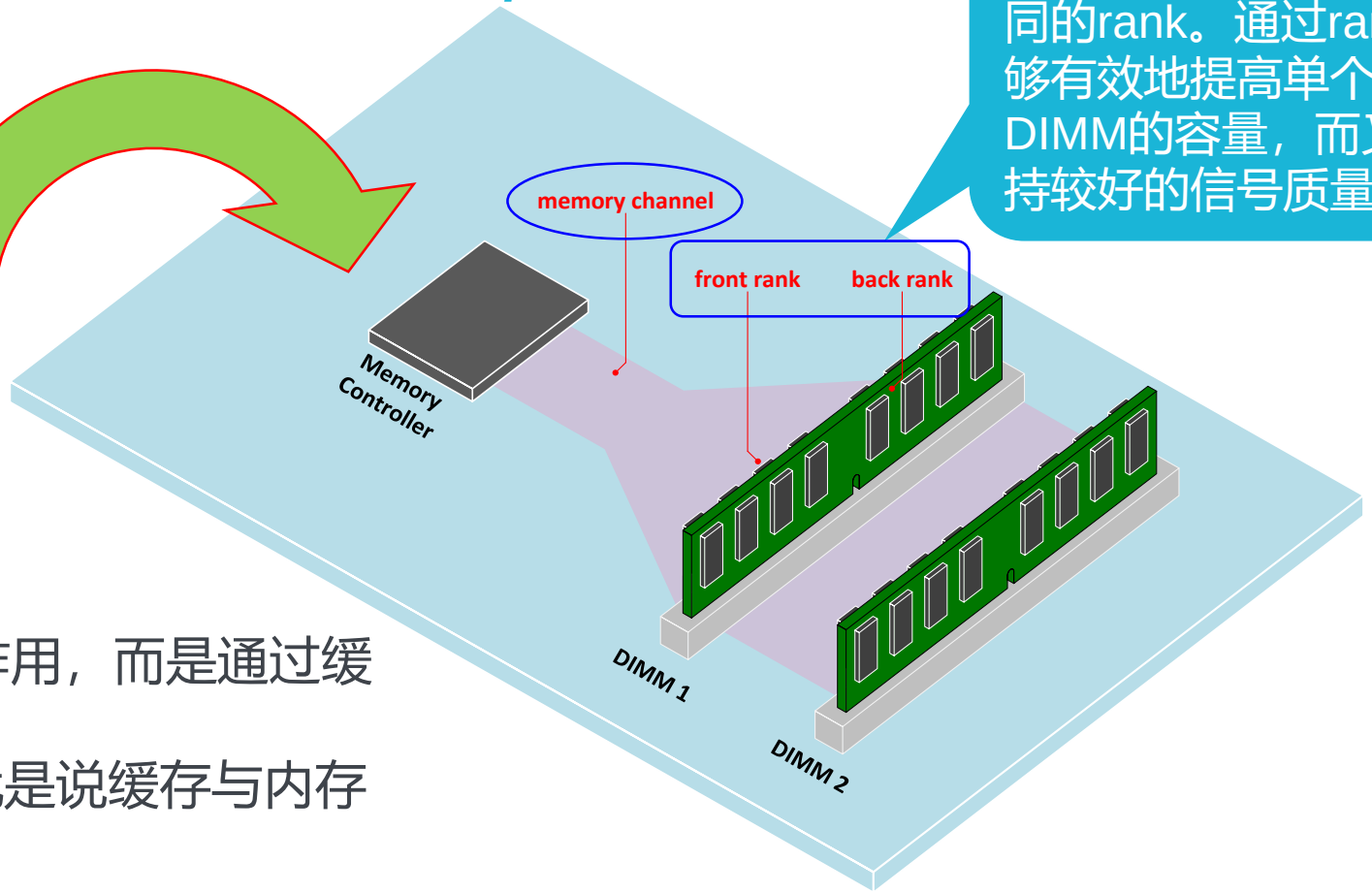


DDR3 Read and Write Burst

内存的组织方式

标准计算机系统：UDIMM，2 DIMM per channel， 2 ranks per DIMM





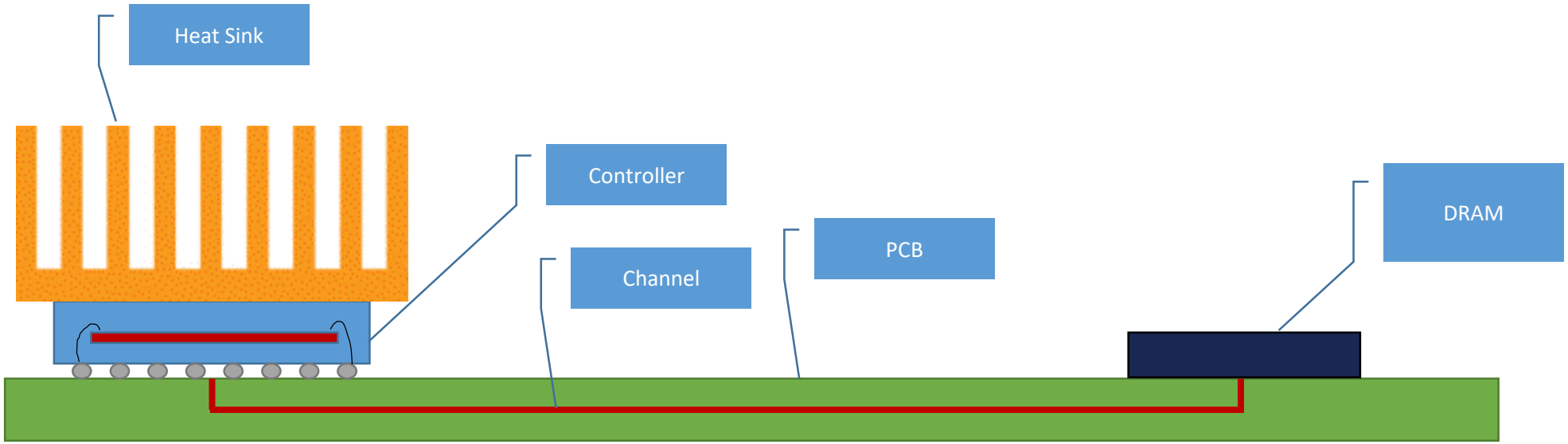
通过片选信号来区分不同的rank。通过rank能够有效地提高单个DIMM的容量，而又保持较好的信号质量

- CPU Core并不是直接和内存发生作用，而是通过缓存来和内存发生作用
- Cache Line的大小为64 Byte；也就是说缓存与内存相互作用的最小单位为64 Byte

channel → DIMM → rank → (chip → die → bank group →bank → row → column → n-bit memory cells)

内存的组织方式

嵌入式系统



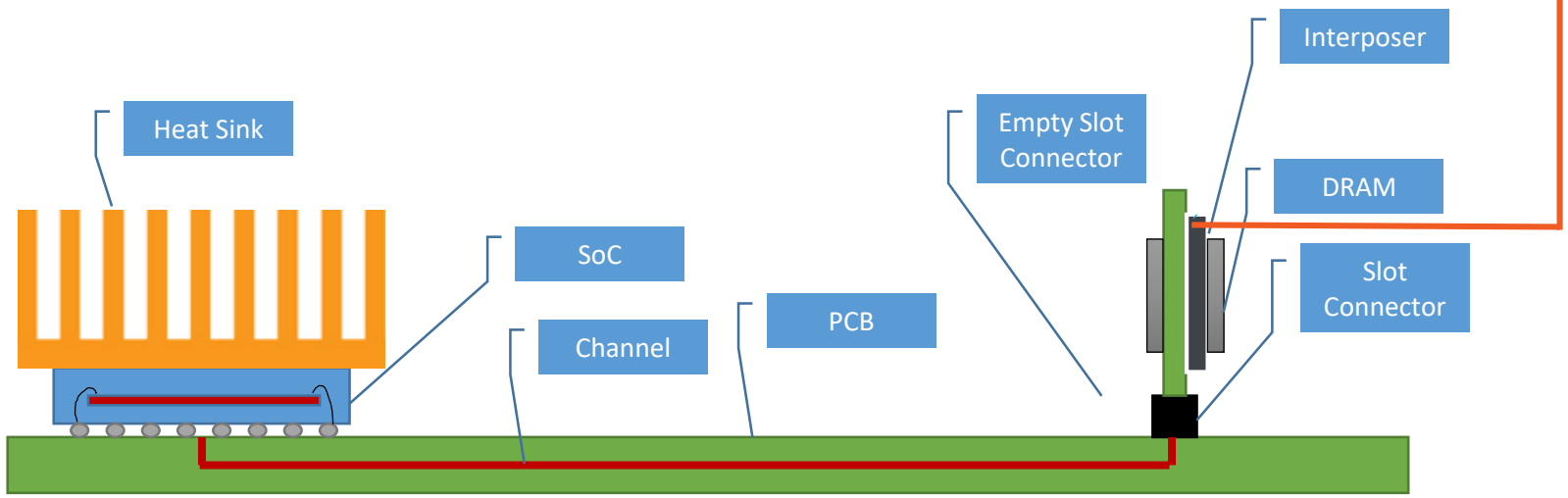
- 内存控制器芯片与DRAM颗粒芯片在同一块PCB上；
- 内存通道的总线宽度根据所选择的内存控制器芯片的不同而不同；

DDR接口的测试挑战

DRAM System Testing

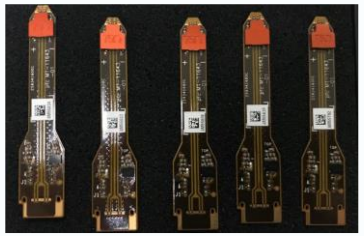
3 Key Challenges Associated with Memory Testing:

1. Memory Signal Access
2. Detect and Qualify the Burst on the Signal
3. Configure and Perform DDR Measurements for Conformance



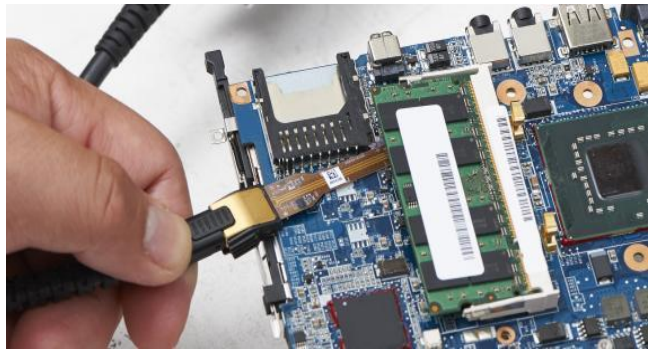
Probing Scheme

TDP7700 Probe and Flexible Probe Tips



Solder-in tips(15GHz)

- P77STFLXB



SMA adapter

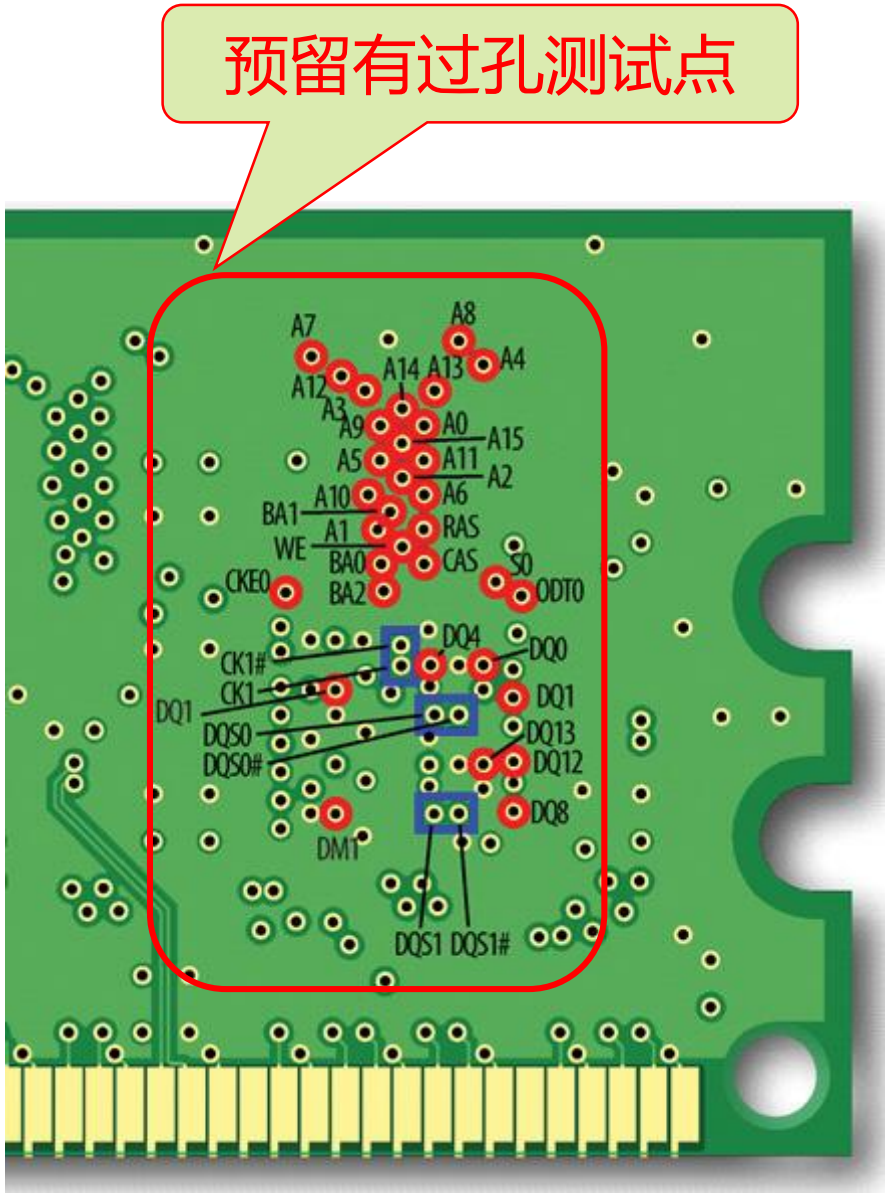
Browser

Solder-in tips
(Most preferred for memory testing)

Probing Scheme

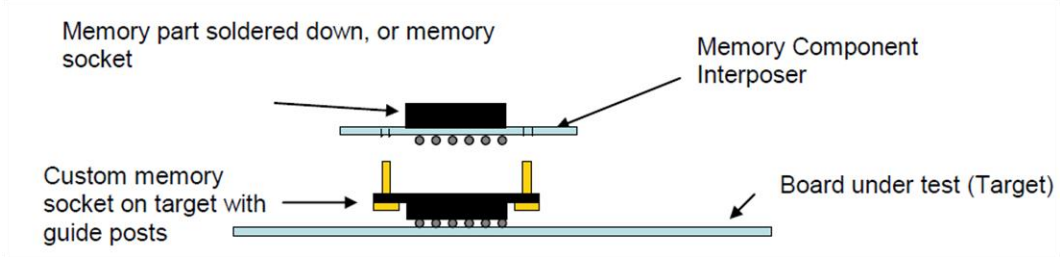
Direct Probing

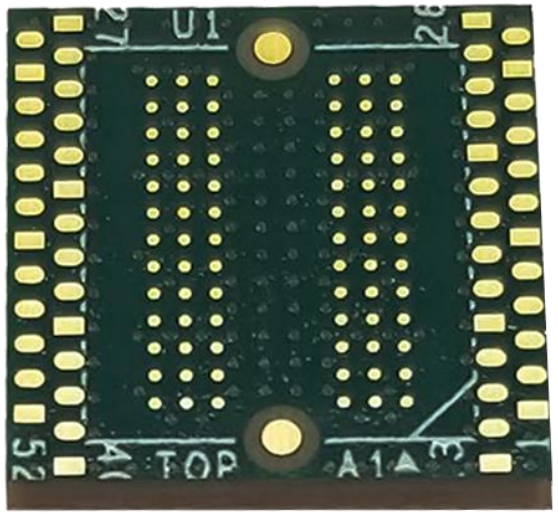
- 计算机系统采用标准化的DIMM，可以使用多种探测解决方案进行探测；
- 嵌入式设计中的通常直接把DRAM芯片焊接在PCB上，而所有的DDR3颗粒均采用BGA封装。*JEDEC的规格定义的测试点为BGA的焊球处*:
  - 在PCB layout时，就通过过孔在背面预留有测试点，这样可以直接点测完全信号的探测；也就是DfT（Design for Test）。
  - 当使用直接探测时，可以得到很好的信号保真度；
  - 但对于PCB正反面都贴有DRAM颗粒，这种方法无能为力



Probing Scheme

BGA Interposer



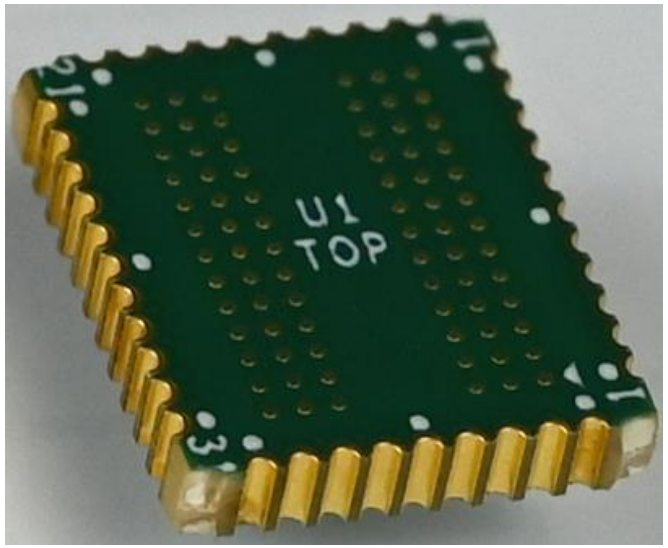


Direct-Attach

- 转接板焊接到待测PCB上；
- DRAM颗粒焊接到转接板上；
- 转接板面积大于DRAM颗粒的面积

Target-Socketed

- 将定制的BGA插座焊接到待测PCB上；
- 通过按压将转接板连接到插座上；
- DRAM颗粒按压到转接板操作上；
- 方便评估不同的DRAM颗粒；
- 方便在信号完整性测试和协议分析之间进行无缝切换

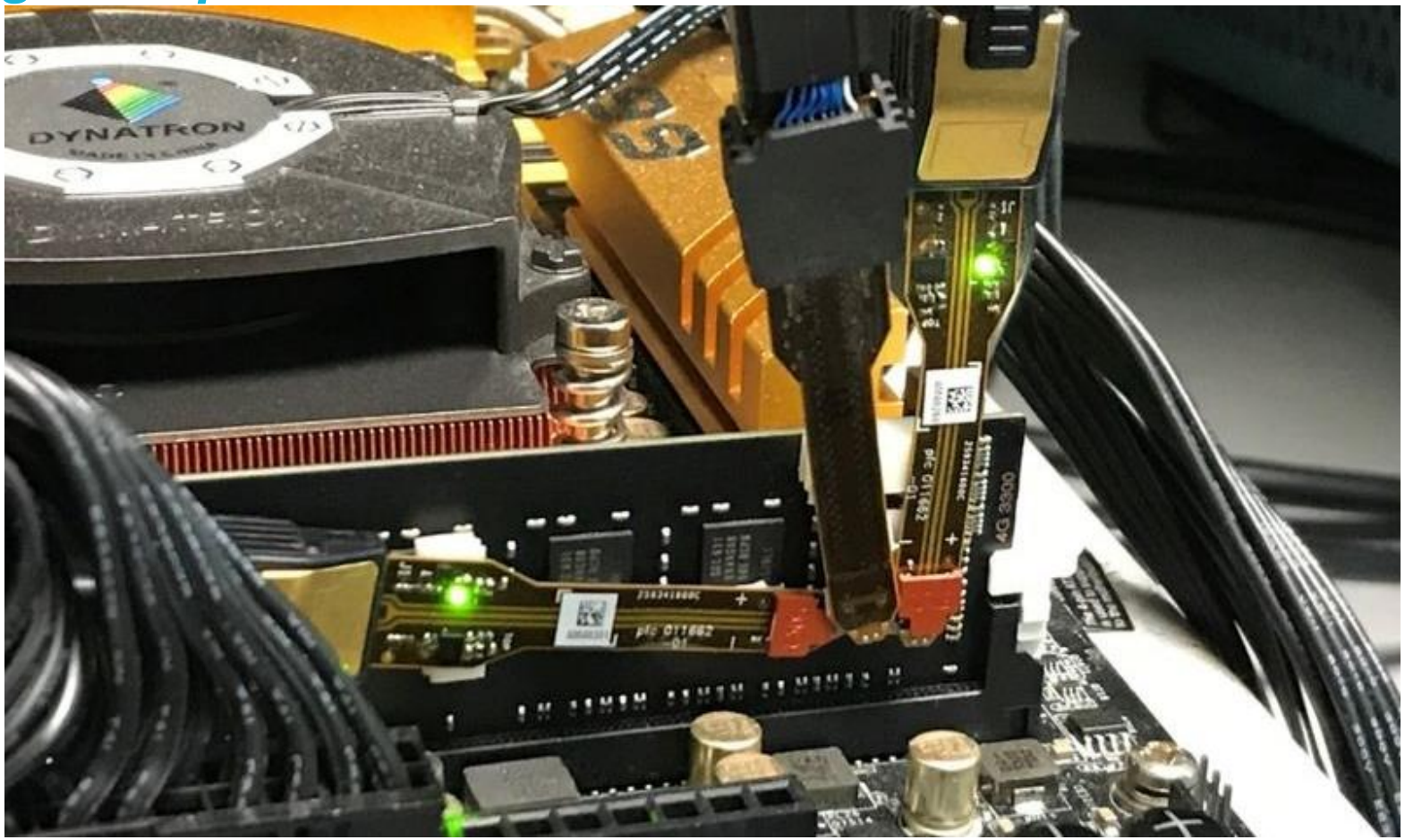


Edge-Probe

- 测试点在转接板的边沿；
- 转接板大小与DRAM颗粒大小相同；
- 适用于PCB空间比较紧张的场合

Probing Scheme

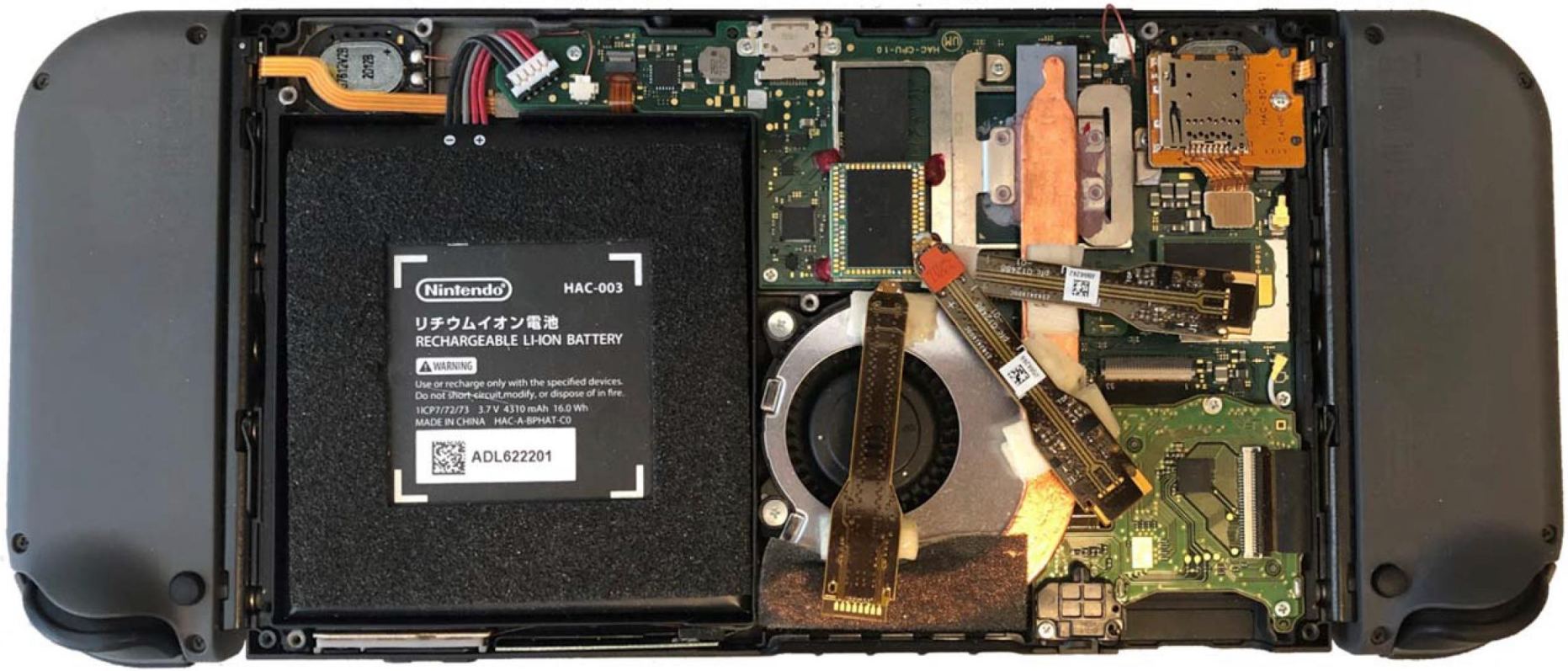
Direct Probing example



DDR3 DIMM + TDP7700 Probe Tips

Probing Scheme

Interposer attach example(1)



LPDDR3 Interposer + P7700 Probe Tip

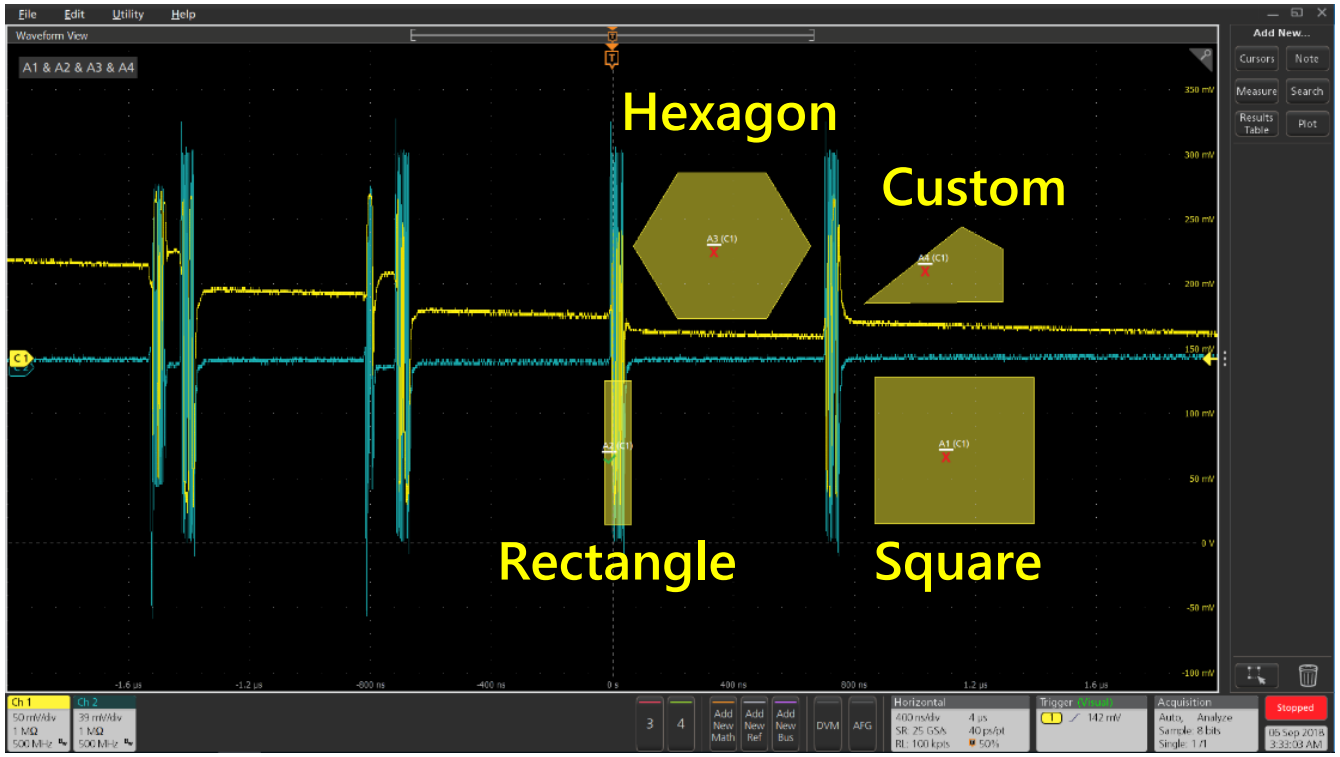
突发识别的方法

读写分离

- 在分析时，需要自动将读突发和写突发分离开来独自进行分析
- 对于读写分离，有若干种方法：
  - DQ/DQS phase alignment：基于读操作和写操作的DQ/DQS相位对齐关系的不同。读操作为边沿对齐，写操作为中心对齐。这种最常用
  - Visual Trigger：可视触发，用户自定义可视触发条件，灵活度非常高
  - CS, Latency + DQ/DQS phase alignment：当有多个rank时，需要通过CS信号来区分是哪一个rank进行读写；
  - Logic State + Burst Latency：通过解析命令信号群组（RAS#-CAS#-WE#）来确定读操作和写操作

Benefits of Visual Trigger for DDR Testing

- Trigger on user specified conditions
- Filter using graphical ‘Areas’
  - In, Out or Don’t Care for each Area
- Standard shapes
  - Rectangle, triangle, trapezoid and hexagon
  - Or build your own custom shapes
  - Areas may be resized or moved after creation
- Used To:
  - Separate Read bursts from Write Bursts
  - Look for pattern dependencies
  - Enable Persistence of Eye diagrams



泰克的测试解决方案——6-DBDDR3

- 覆盖所有DDR3测试项
- 需手动进行测试配置
- 需手动添加测试项

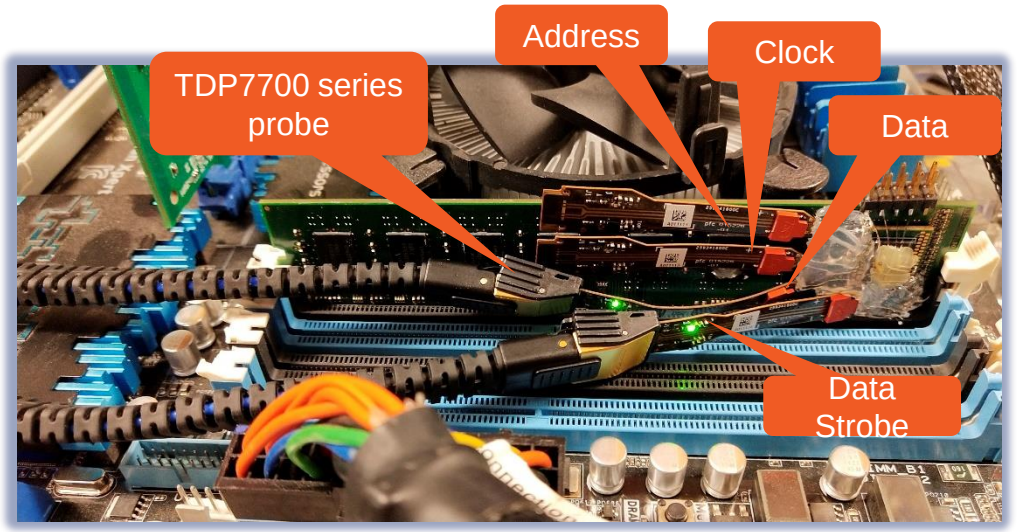
6-DBDDR3 Features

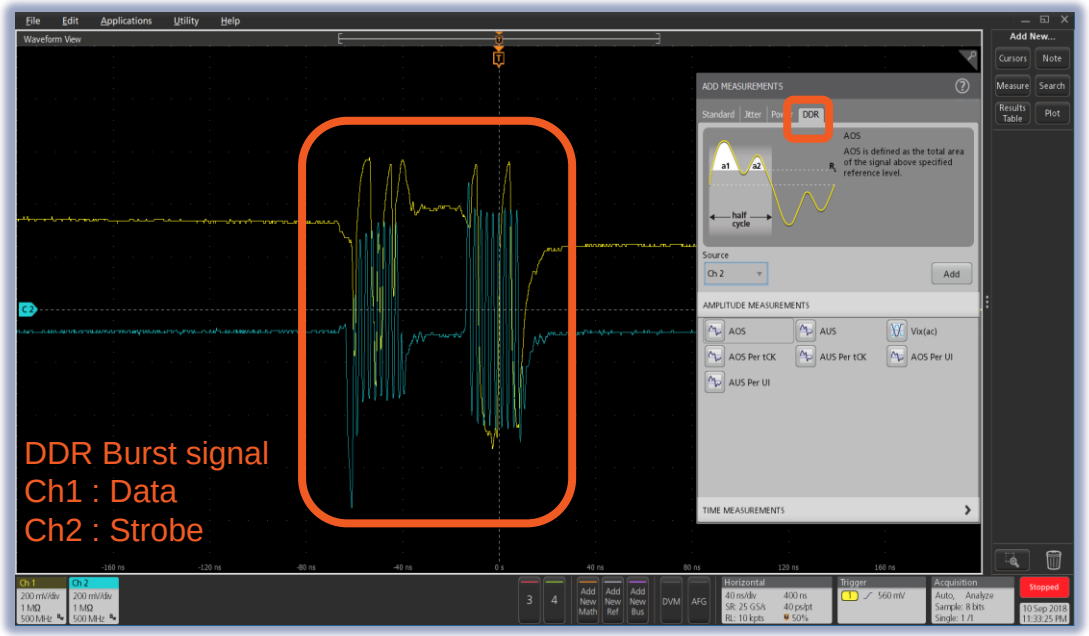
- Supported Data rate (MT/s)
  - 800, 1066, 1333, 1600, 1866 & 2133

- Analyze Timing and Amplitude characteristics of data exchange between memory and memory controller

- TDP77XX probes enable probing at the pins of the memory chip using P77STFLXA flextips adapters

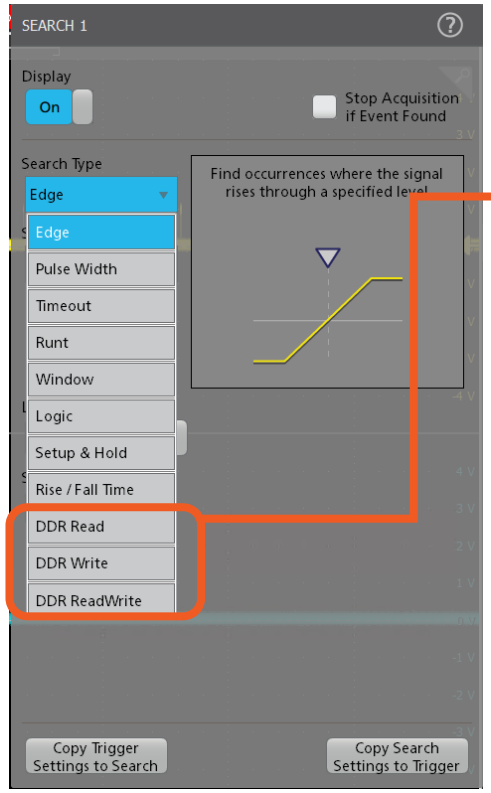
- Perform measurements on the region of interest identified as a Read or a Write ‘Burst’





Simple 4-Step Workflow…

Step 1: Define Search

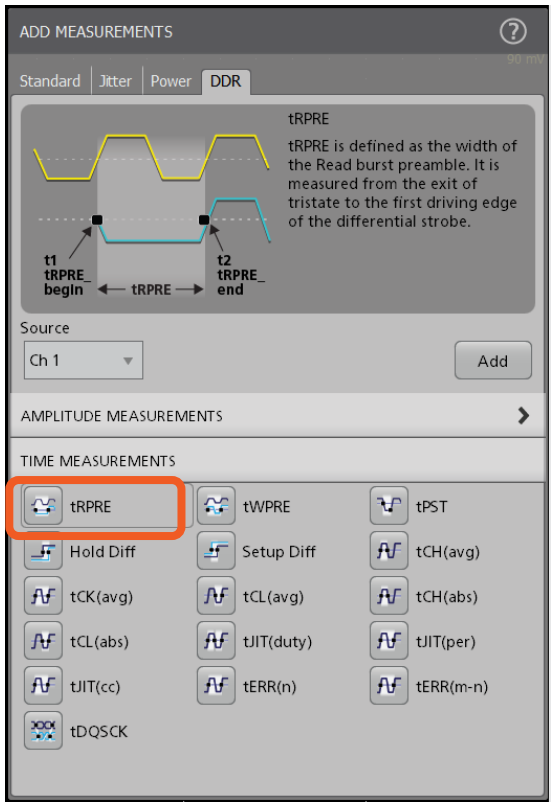


Select DDR-specific Search Type
- Read
- Write
- Read/Write

Step 2: Configure Search

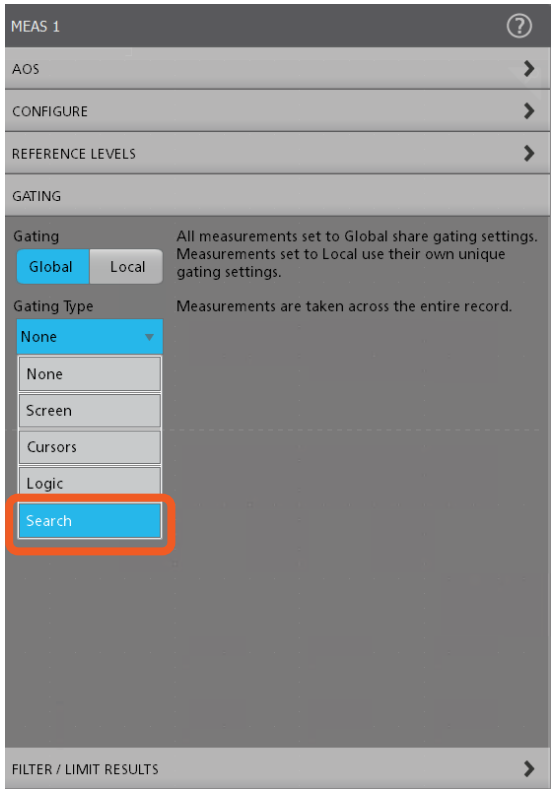
- Define Data (DQ) and Strobe (DQS) inputs
- Select DDR3 or LPDDR3
- Select DUT's data rate

Step 3: Select Measurement



Choose from DDR3 measurements
There are two groups:
- Amplitude Measurements
- Time Measurements

Step 4: Define Gating



Configure the measurement
Define Search as gating to perform measurements on valid regions

DDR3测试项

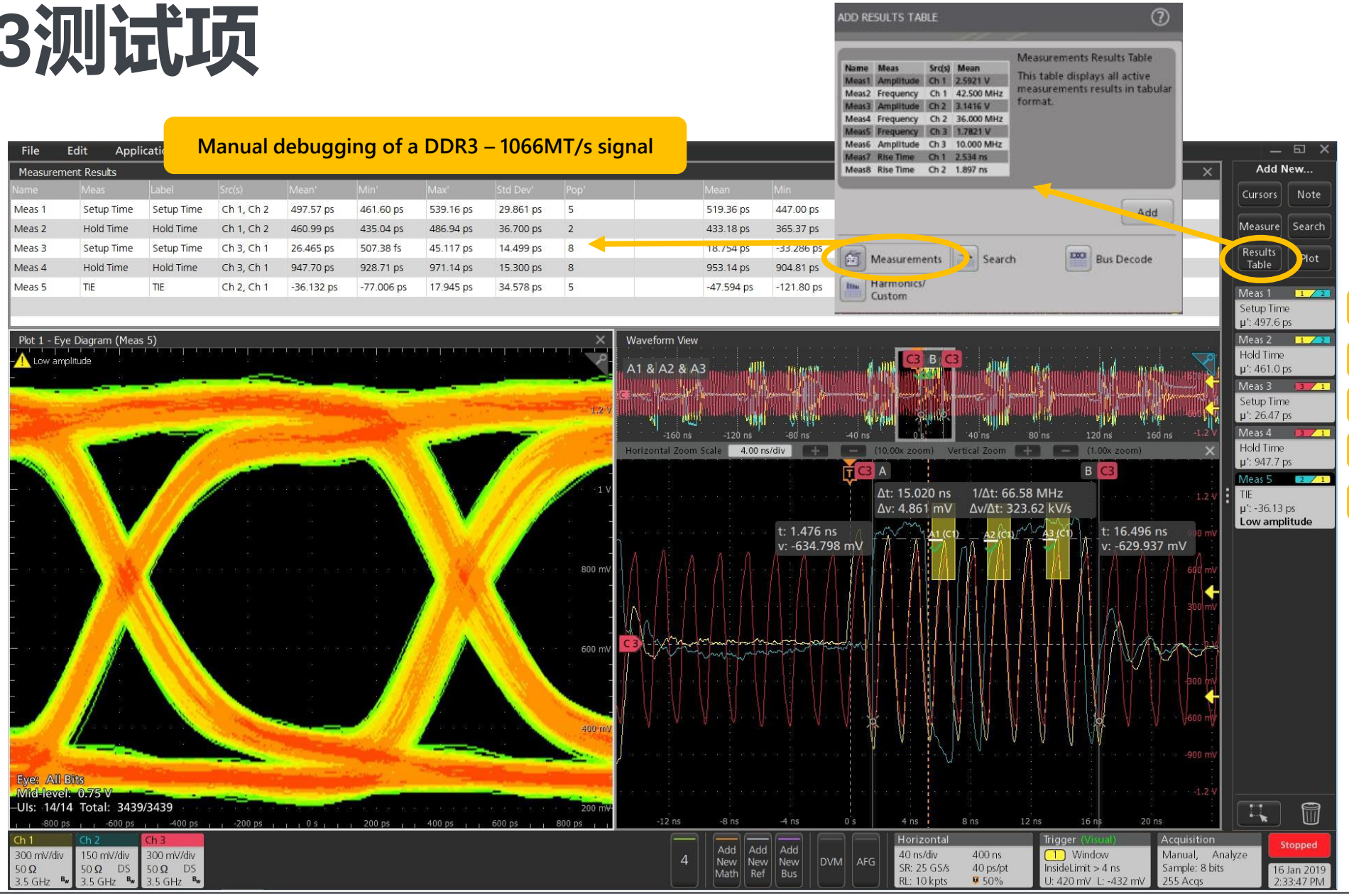
Amplitude Analysis measurements	
AOS	The total area of the signal above the specified reference level.
AUS	The total area of the signal below the specified reference level.
Vix(ac)	The differential input cross-point voltage measured from the actual crossover voltage and its complement signal to a designated reference voltage. This is measured on single ended signal.
AOS Per tCK	The total area of the signal that crosses the specified reference level calculated over consecutive periods. It is applicable to clock and address/command waveforms only.
AUS Per tCK	The total area of the signal that crosses the specified reference level calculated over consecutive periods. It is applicable to clock and address/command waveforms only.
AOS Per UI	The total area of the signal that crosses the specified reference level calculated over consecutive unit intervals. It is applicable to data and data strobe waveforms only.
AUS Per UI	The total area of the signal that crosses the specified reference level calculated over consecutive unit intervals. It is applicable to data and data strobe waveforms only.
Timing Analysis measurements	
tRPRE	The width of the Read burst preamble. This is measured from the exit of tristate to the first driving edge of the differential strobe.
tWPRE	The width of the Write burst preamble. It is measured from the exit of tristate to the first driving edge of the differential strobe.
tPST	The width of Read or Write burst' postamble. It is measured from the last falling edge crossing the mid reference level to the start of an undriven state (as measured by a rising trend per JEDEC specification).
Hold Diff	The elapsed time between the designated edge of the single ended waveform and the designated edge of a differential waveform. The measurement uses the closest single ended waveform edge to the differential waveform edge that falls within the range limits.
Setup Diff	The elapsed time between the designated edge of a single ended waveform and when the differential waveform crosses its own voltage reference level. The measurement uses the closest single ended waveform edge to the differential waveform edge that falls within the range limits.
tCH(avg)	The average high pulse width calculated across a sliding 200 cycle window of consecutive high pulses.
tCK(avg)	The average clock period across a sliding 200-cycle window.
tCL(avg)	The average low pulse width calculated across a sliding 200 cycle window of consecutive low pulses.
tCH(abs)	The high pulse width of the differential clock signal. It is the amount of time the waveform remains above the mid reference voltage level.
tCL(abs)	The low pulse width of the differential clock signal. It is the amount of time the waveform remains below the mid reference voltage level.
tJIT(duty)	The largest elapsed time between tCH and tCH(avg) or tCL and tCL(avg) for a 200-cycle window.
tJIT(per)	The largest elapsed time between tCK and tCK(avg) for a 200-cycle sliding window.
tJIT(cc)	The absolute difference in clock period between two consecutive clock cycles.
tERR(n)	The cumulative error across multiple consecutive cycles from tCK(avg). It measures time difference between the sum of clock period for a 200-cycle window to n times tCK(avg).
tERR(m-n)	The cumulative error across multiple consecutive cycles from tCK(avg). It measures the time difference between the sum of clock periods for a 200-cycle window to n times tCK(avg).
tDQSCK	The strobe output access time from differential clock. It is measured between the rising edge of clock before or after the differential strobe Read preamble time. The edge locations are determined by the mid-reference voltage levels.
tCMD-CMD	measures the elapsed time between two logic states
tCKSRE	measures the valid clock cycles required after Self Refresh Entry (SRE) command. Changing the input clock frequency or the supply voltage is permissible only after tCKSRE time when the SRE command is registered.
tCKSRX	measures the valid clock cycles required before the Self Refresh Exit (SRX) command. Changing the input clock frequency or the supply voltage is permissible provided the new clock frequency or supply voltage is stable for the tCKSRX time prior to SRX command

DDR3测试项

举例：测试幅度

DDR3测试项

Manual debugging of a DDR3 – 1066MT/s signal



tDS

tDH

tDSS

tDSH

DQ Eye

Test Results

Displays detailed results

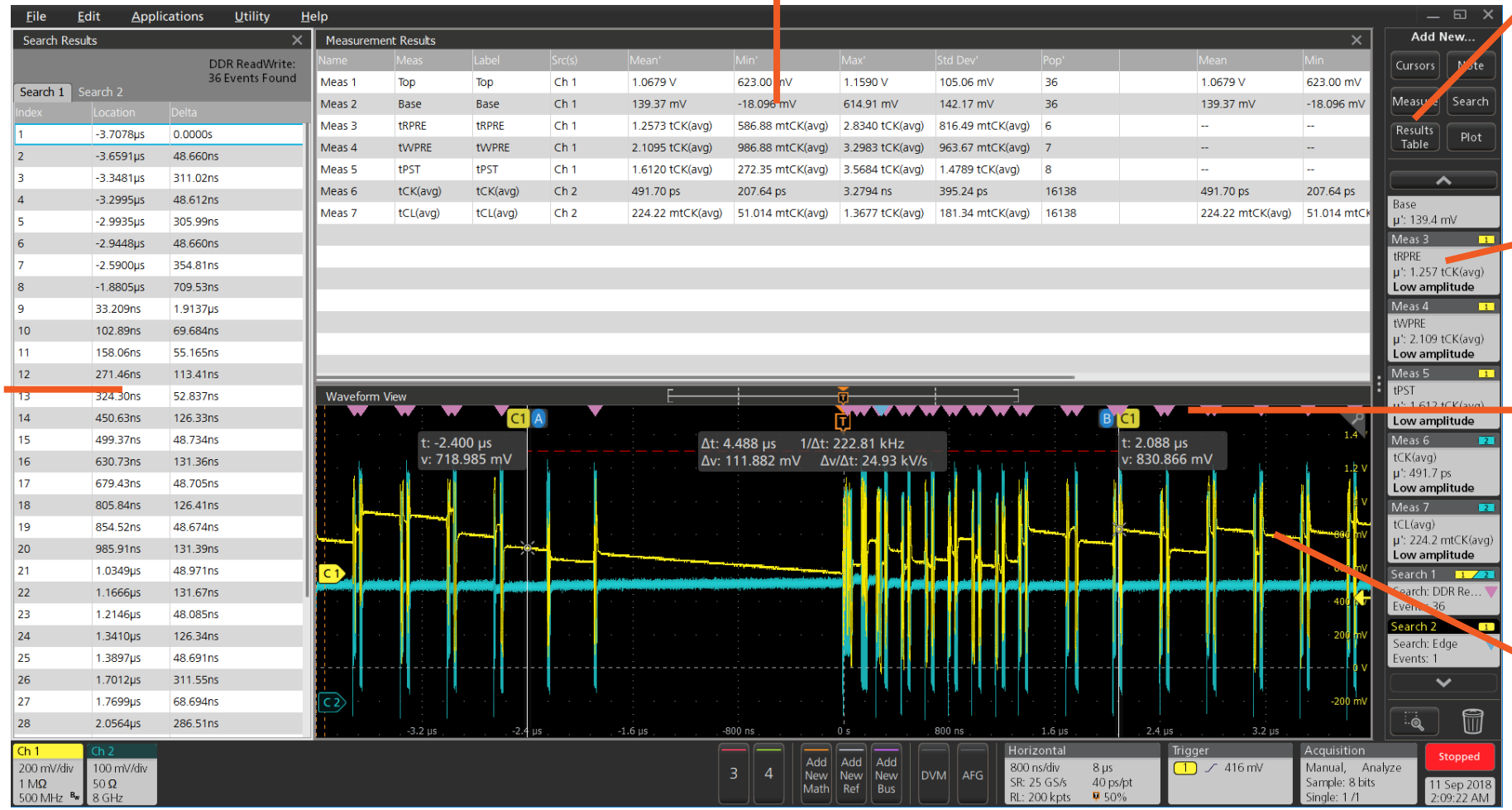
Click on Results Table button

Get a view of search results. Easily navigate through the qualified searches

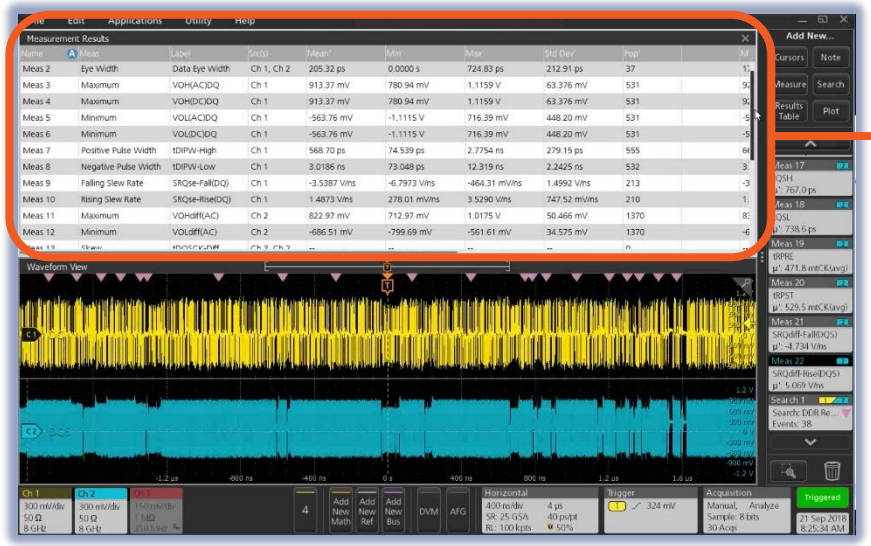
DDR3 measurements

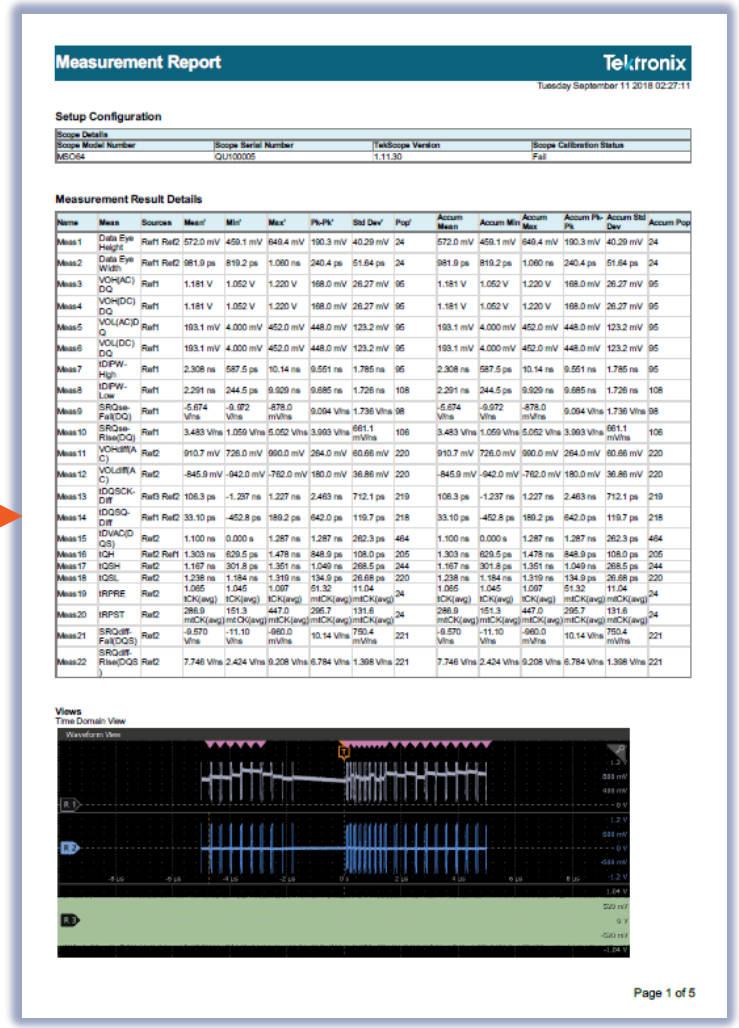
Valid bursts searched and marked indicated by pink triangles

DDR3 waveform
Ch1: DQ
Ch2: DQS



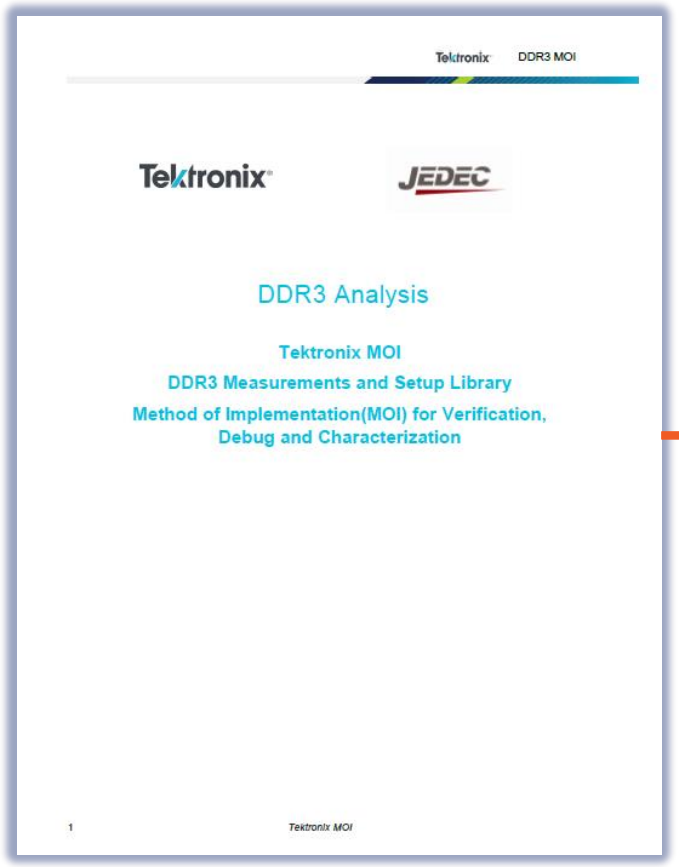
Reports

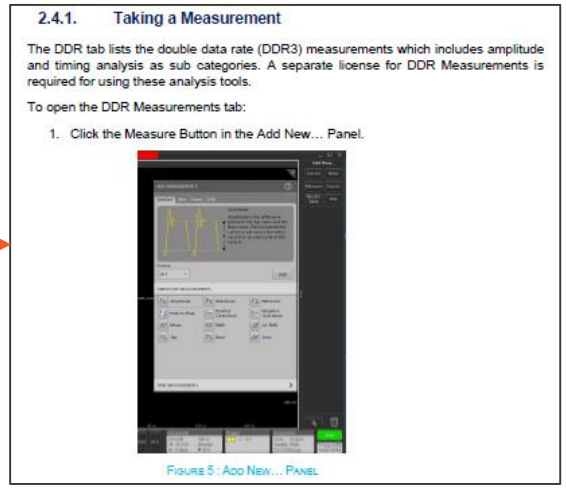




- Analysis results are compiled into HTML & PDF report enabling easy report management and distribution
- Report includes:
  - Measurement results and statistics
  - Instrument configuration summary
  - Plot images
- Perform single run or statistical analysis across user defined population count

Detailed MOI Document





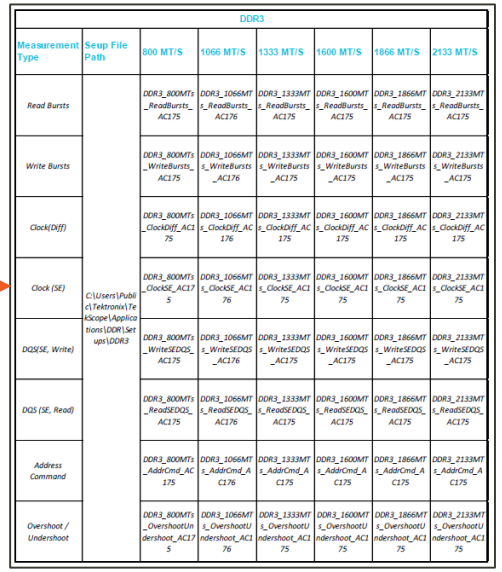
2.4.1. Taking a Measurement

The DDR tab lists the double data rate (DDR3) measurements which includes amplitude and timing analysis as sub categories. A separate license for DDR Measurements is required for using these analysis tools.

To open the DDR Measurements tab:

1. Click the Measure Button in the Add New... Panel.

FIGURE 5 : ADD NEW... PANEL

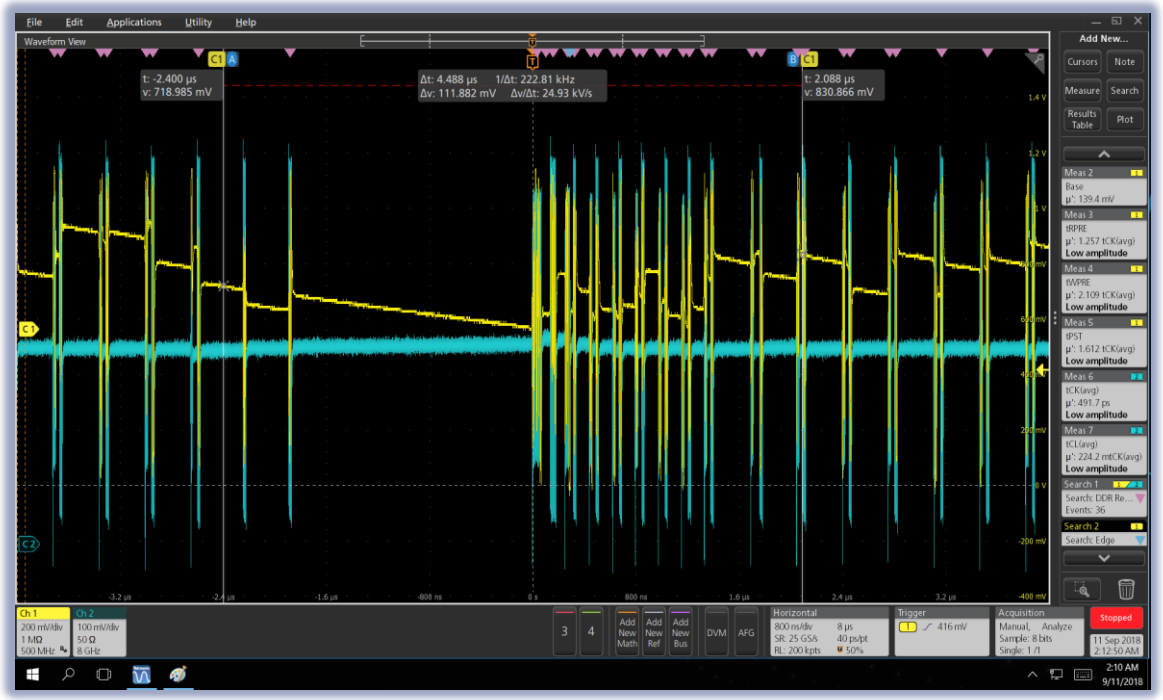


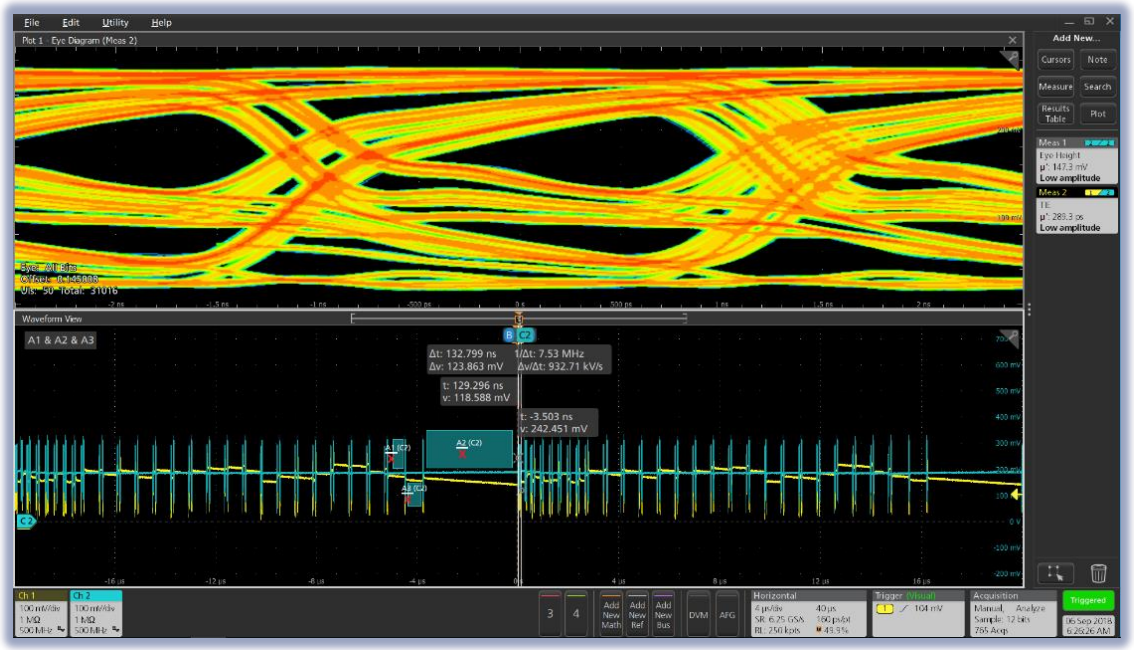
DDR3							
Measurement Type	Seup File Path	800 MT/S	1066 MT/S	1333 MT/S	1600 MT/S	1866 MT/S	2133 MT/S
Read Bursts	C:\Users\Public\Tektronix\TekScope\Applications\DDR\Setups\DDR3	DDR3_800MTs_ReadBursts_AC175	DDR3_1066MTs_ReadBursts_AC176	DDR3_1333MTs_ReadBursts_AC175	DDR3_1600MTs_ReadBursts_AC175	DDR3_1866MTs_ReadBursts_AC175	DDR3_2133MTs_ReadBursts_AC175
Write Bursts		DDR3_800MTs_WriteBursts_AC175	DDR3_1066MTs_WriteBursts_AC176	DDR3_1333MTs_WriteBursts_AC175	DDR3_1600MTs_WriteBursts_AC175	DDR3_1866MTs_WriteBursts_AC175	DDR3_2133MTs_WriteBursts_AC175
Clock(Diff)		DDR3_800MTs_ClockDiff_AC175	DDR3_1066MTs_ClockDiff_AC176	DDR3_1333MTs_ClockDiff_AC175	DDR3_1600MTs_ClockDiff_AC175	DDR3_1866MTs_ClockDiff_AC175	DDR3_2133MTs_ClockDiff_AC175
Clock (SE)		DDR3_800MTs_ClockSE_AC175	DDR3_1066MTs_ClockSE_AC176	DDR3_1333MTs_ClockSE_AC175	DDR3_1600MTs_ClockSE_AC175	DDR3_1866MTs_ClockSE_AC175	DDR3_2133MTs_ClockSE_AC175
DQS(SE, Write)		DDR3_800MTs_WriteSEDQS_AC175	DDR3_1066MTs_WriteSEDQS_AC176	DDR3_1333MTs_WriteSEDQS_AC175	DDR3_1600MTs_WriteSEDQS_AC175	DDR3_1866MTs_WriteSEDQS_AC175	DDR3_2133MTs_WriteSEDQS_AC175
DQS (SE, Read)		DDR3_800MTs_ReadSEDQS_AC175	DDR3_1066MTs_ReadSEDQS_AC176	DDR3_1333MTs_ReadSEDQS_AC175	DDR3_1600MTs_ReadSEDQS_AC175	DDR3_1866MTs_ReadSEDQS_AC175	DDR3_2133MTs_ReadSEDQS_AC175
Address Command		DDR3_800MTs_AddrCmd_AC175	DDR3_1066MTs_AddrCmd_AC176	DDR3_1333MTs_AddrCmd_AC175	DDR3_1600MTs_AddrCmd_AC175	DDR3_1866MTs_AddrCmd_AC175	DDR3_2133MTs_AddrCmd_AC175
Overshoot / Undershoot		DDR3_800MTs_OvershootUndershoot_AC175	DDR3_1066MTs_OvershootUndershoot_AC176	DDR3_1333MTs_OvershootUndershoot_AC175	DDR3_1600MTs_OvershootUndershoot_AC175	DDR3_1866MTs_OvershootUndershoot_AC175	DDR3_2133MTs_OvershootUndershoot_AC175

- DUT Settings
- Oscilloscope Settings
  - Horizontal, Vertical and Trigger settings
- Measurement Source Settings Table
- How to make a manual measurement
- Recalling a built-in demo session file
- Reference to setup files
- DDR Measurements Overview
  - Read Burst, Write Burst, Clock, DQS, Address Command, Overshoot and Undershoot, Digital measurements

Benefits of 6-DJA

- Enables Jitter and Eye diagram profiling





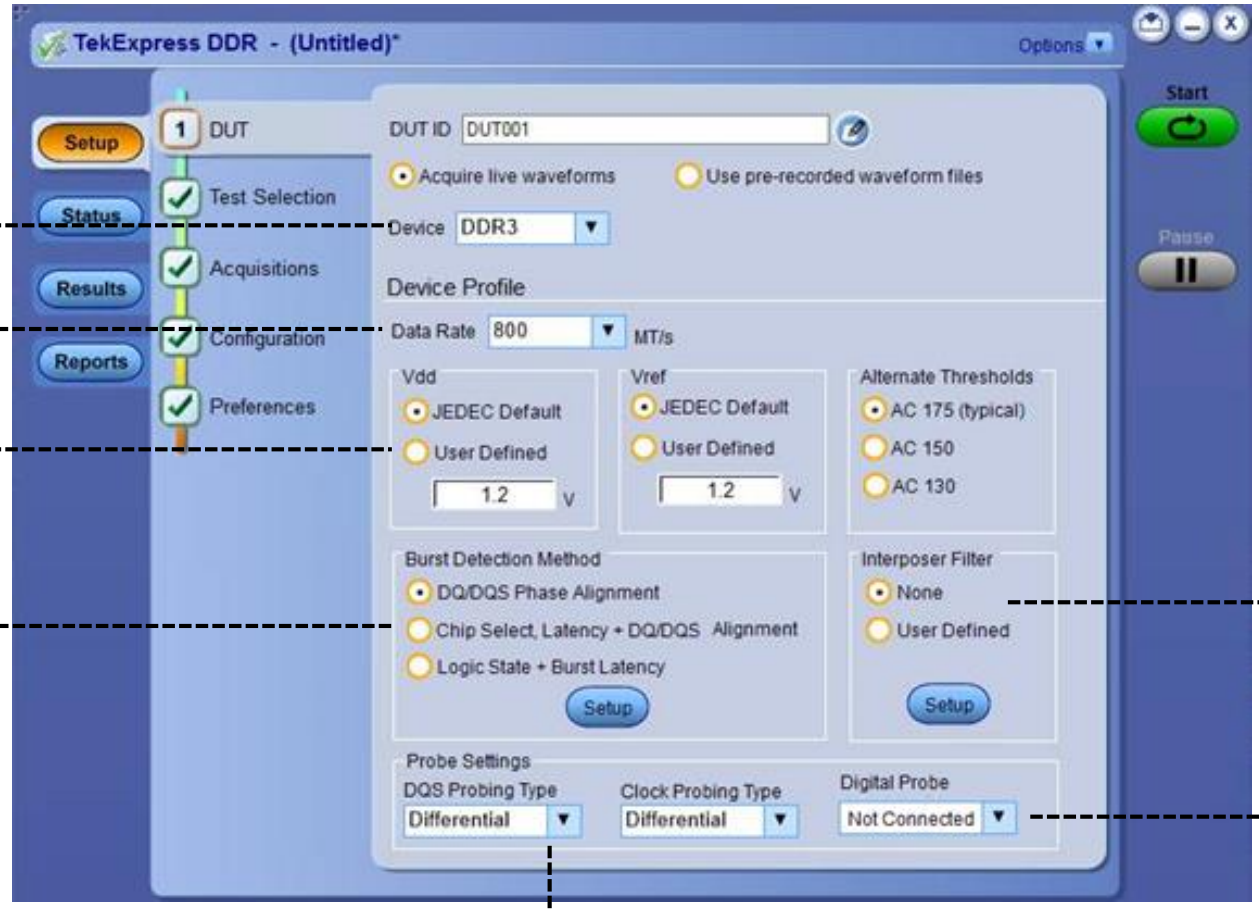
- Enables Jitter and Eye diagram profiling

泰克的测试解决方案——6-CMDDR3

- 覆盖所有DDR3测试项
- 自动进行测试配置
- 自动添加测试项

6-CMDDR3 – TekExpress DDR Solution

DUT PANEL



DDR3
LPDDR3

Speed Grades

Voltage Levels

Burst Detection Methods

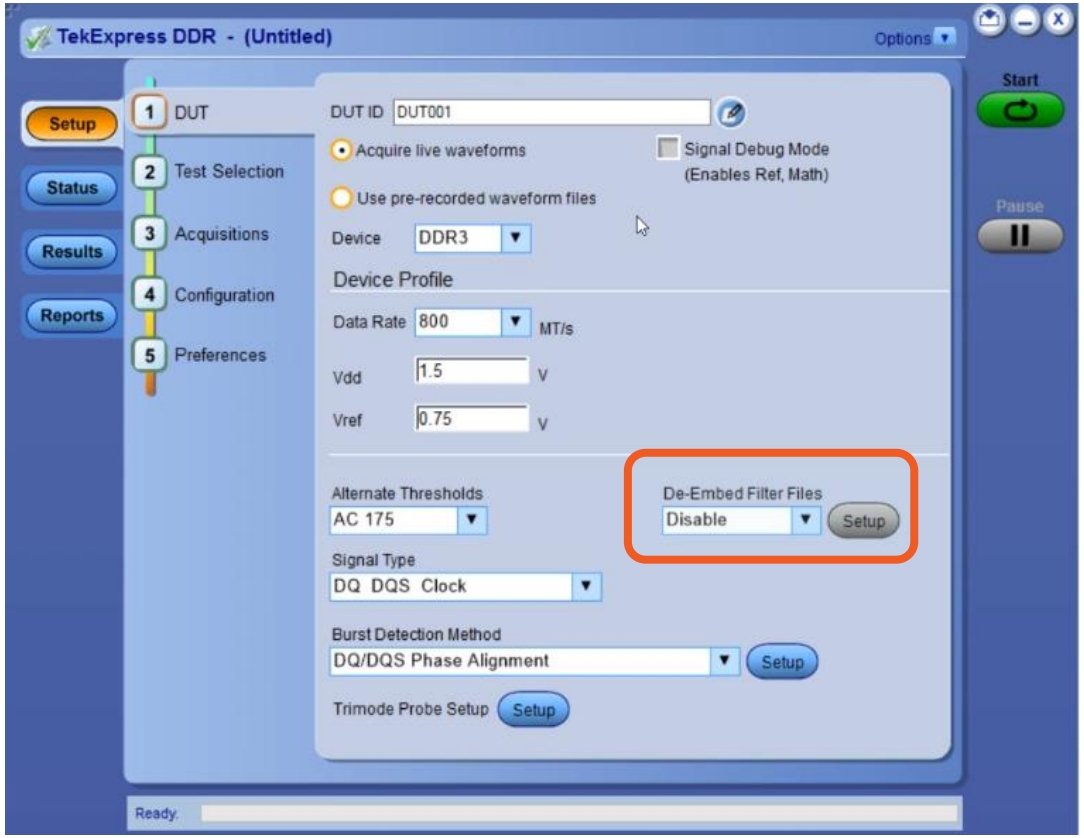
De-embed support using .flt file bundled with the app. User can provide their own .flt file

Support for TLP058 Logic probes to probe CAS,RAS, CS & WE lines

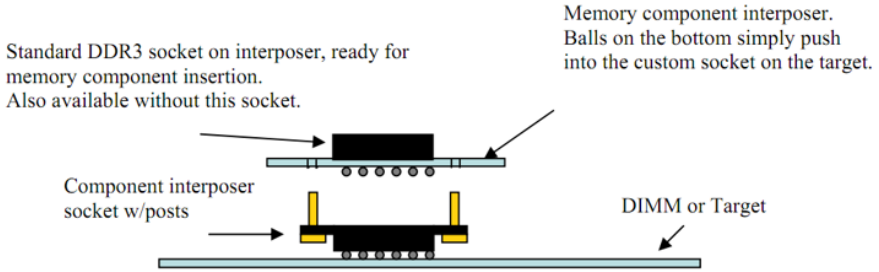
Analog probes for DQ, DQS and Clock

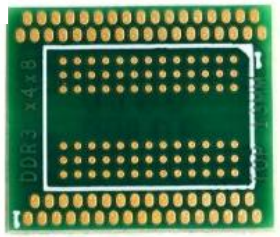
6-CMDDR3 – TekExpress DDR Solution

Support for Filter Files



Technology	Package / Form Factor
DDR3	Socketed – 78 ball/ 96 ball Solder-down – 78 ball/ 96 ball Edge Probe – 78 ball/ 96 ball DIMM Interposer for MSO SO-DIMM Interposer for MSO
LPDDR3	Socketed – 216 ball Solder-down – 178 ball/221 ball



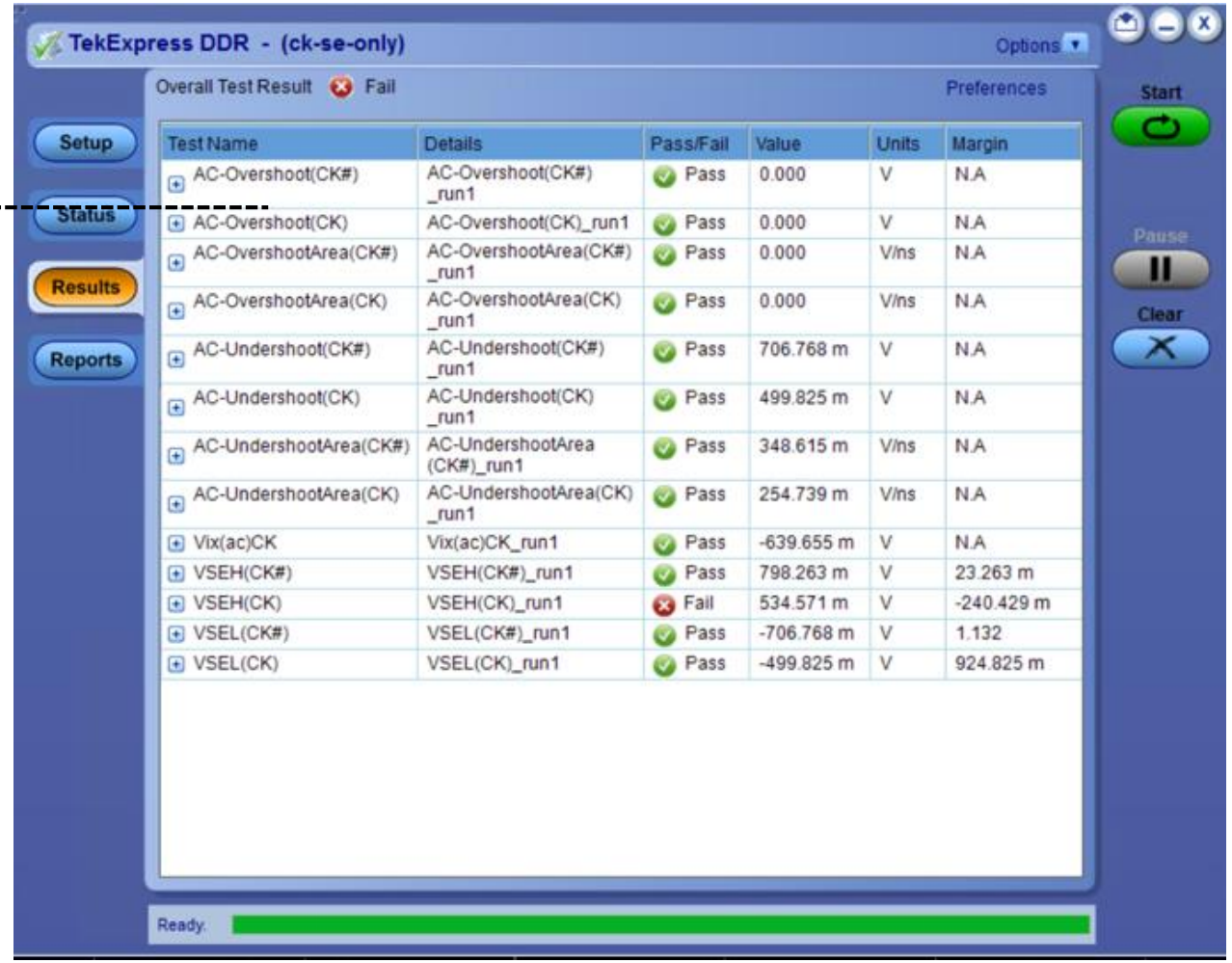


Interposers from Nexus Technologies

6-CMDDR3 – TekExpress DDR Solution

Results Panel

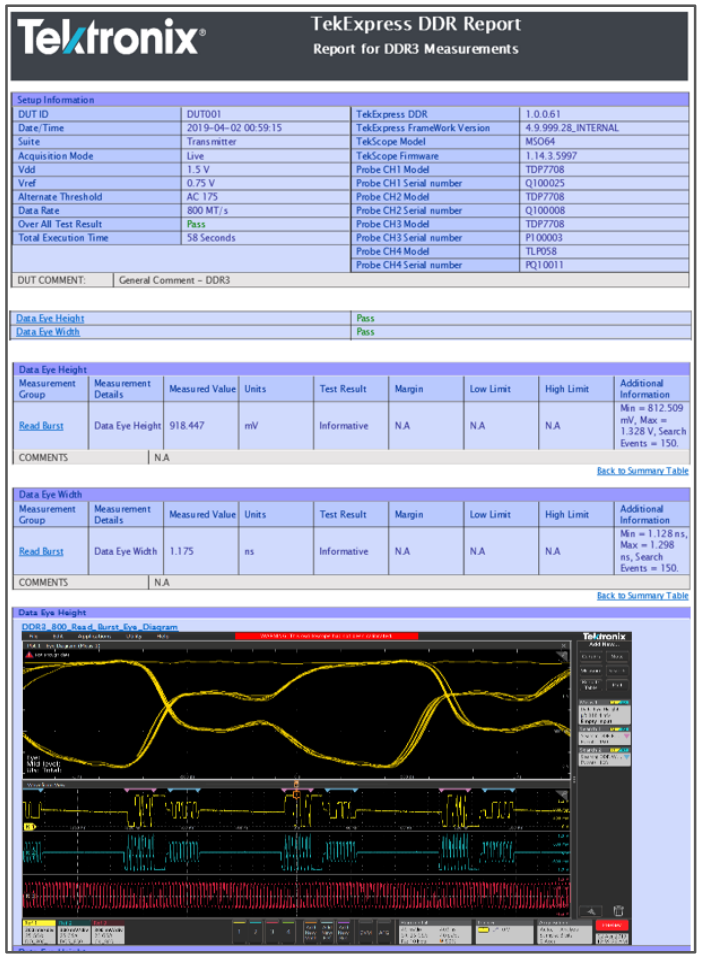
Detailed results with pass/fail, limits and margins



Test Name	Details	Pass/Fail	Value	Units	Margin
AC-Overshoot(CK#)	AC-Overshoot(CK#)_run1	Pass	0.000	V	N.A
AC-Overshoot(CK)	AC-Overshoot(CK)_run1	Pass	0.000	V	N.A
AC-OvershootArea(CK#)	AC-OvershootArea(CK#)_run1	Pass	0.000	V/ns	N.A
AC-OvershootArea(CK)	AC-OvershootArea(CK)_run1	Pass	0.000	V/ns	N.A
AC-Undershoot(CK#)	AC-Undershoot(CK#)_run1	Pass	706.768 m	V	N.A
AC-Undershoot(CK)	AC-Undershoot(CK)_run1	Pass	499.825 m	V	N.A
AC-UndershootArea(CK#)	AC-UndershootArea(CK#)_run1	Pass	348.615 m	V/ns	N.A
AC-UndershootArea(CK)	AC-UndershootArea(CK)_run1	Pass	254.739 m	V/ns	N.A
Vix(ac)CK	Vix(ac)CK_run1	Pass	-639.655 m	V	N.A
VSEH(CK#)	VSEH(CK#)_run1	Pass	798.263 m	V	23.263 m
VSEH(CK)	VSEH(CK)_run1	Fail	534.571 m	V	-240.429 m
VSEL(CK#)	VSEL(CK#)_run1	Pass	-706.768 m	V	1.132
VSEL(CK)	VSEL(CK)_run1	Pass	-499.825 m	V	924.825 m

6-CMDDR3 – TekExpress DDR Solution

Reports



TekExpress DDR Report
Report for DDR3 Measurements

Setup Information			
DUT ID	DUT001	TekExpress DDR	1.0.0.61
Date/Time	2019-04-02 00:59:15	TekExpress FrameWork Version	4.9.999.28_INTERNAL
Suite	Transmitter	TekScope Model	MSO64
Acquisition Mode	Live	TekScope Firmware	1.14.3.5997
Vdd	1.5 V	Probe CH1 Model	TDP7708
Vref	0.75 V	Probe CH1 Serial number	Q100025
Alternate Threshold	AC 175	Probe CH2 Model	TDP7708
Data Rate	800 MT/s	Probe CH2 Serial number	Q100008
Over All Test Result	Pass	Probe CH3 Model	TDP7708
Total Execution Time	58 Seconds	Probe CH3 Serial number	P100003
		Probe CH4 Model	TLP058
		Probe CH4 Serial number	PQ10011
DUT COMMENT:	General Comment – DDR3		

Data Eye Height	Pass
Data Eye Width	Pass

Data Eye Height

Measurement Group	Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Additional Information
Read Burst	Data Eye Height	918.447	mV	Informative	N.A	N.A	N.A	Min = 812.509 mV, Max = 1.328 V, Search Events = 150.
COMMENTS	N.A							

Back to Summary Table

Data Eye Width

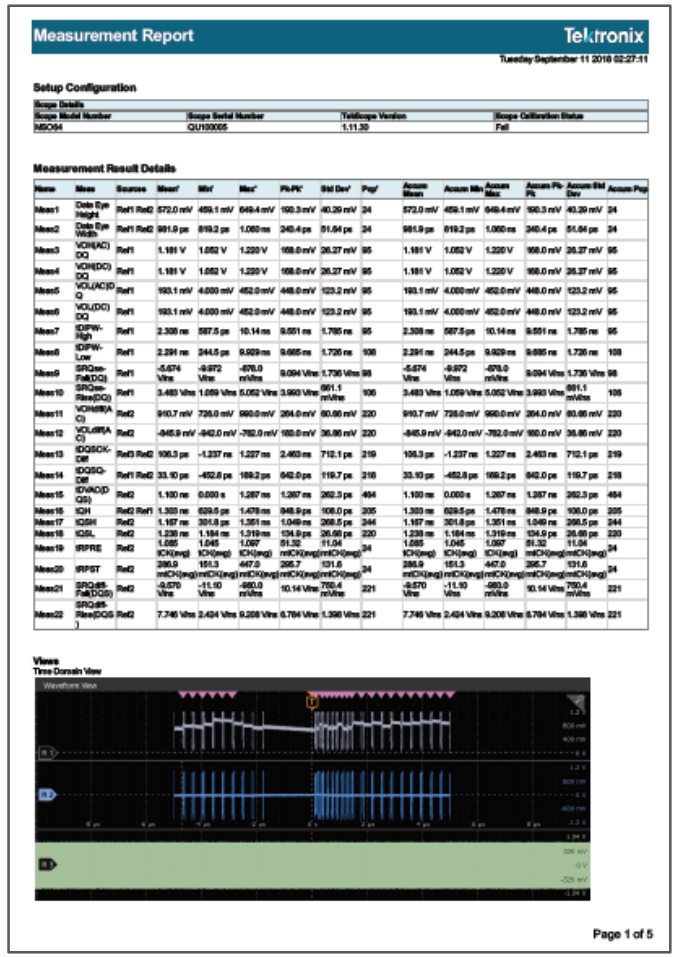
Measurement Group	Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Additional Information
Read Burst	Data Eye Width	1.175	ns	Informative	N.A	N.A	N.A	Min = 1.128 ns, Max = 1.298 ns, Search Events = 150.
COMMENTS	N.A							

Back to Summary Table

Data Eye Height

DDR3_800_Read_Burst_Eye_Diagram

TekExpress automated test report file with detailed test results, setup, margins and test images



Measurement Report

Tektronix

Tuesday September 11 2018 02:27:11

Setup Configuration

Scope Details			
Scope Model Number	Scope Serial Number	TekScope Version	Scope Calibration Status
MSO64	QU100005	1.11.30	Fail

Measurement Result Details

Name	Meas	Sources	Mean	Min	Max	Pk-Pk	Std Dev	Pop	Accum Mean	Accum Min	Accum Max	Accum Pk-Pk	Accum Std Dev	Accum Pop
Meas1	Data Eye Height	Ref1 Ref2	572.0 mV	459.1 mV	649.4 mV	190.3 mV	40.29 mV	24	572.0 mV	459.1 mV	649.4 mV	190.3 mV	40.29 mV	24
Meas2	Data Eye Width	Ref1 Ref2	981.9 ps	819.2 ps	1.060 ns	240.4 ps	51.64 ps	24	981.9 ps	819.2 ps	1.060 ns	240.4 ps	51.64 ps	24
Meas3	VOH(AC) DQ	Ref1	1.161 V	1.052 V	1.220 V	168.0 mV	26.27 mV	95	1.161 V	1.052 V	1.220 V	168.0 mV	26.27 mV	95
Meas4	VOH(DC) DQ	Ref1	1.161 V	1.052 V	1.220 V	168.0 mV	26.27 mV	95	1.161 V	1.052 V	1.220 V	168.0 mV	26.27 mV	95
Meas5	VOL(AC)DQ	Ref1	193.1 mV	4.000 mV	452.0 mV	448.0 mV	123.2 mV	95	193.1 mV	4.000 mV	452.0 mV	448.0 mV	123.2 mV	95
Meas6	VOL(DC) DQ	Ref1	193.1 mV	4.000 mV	452.0 mV	448.0 mV	123.2 mV	95	193.1 mV	4.000 mV	452.0 mV	448.0 mV	123.2 mV	95
Meas7	tDIPW-High	Ref1	2.308 ns	587.5 ps	10.14 ns	9.551 ns	1.785 ns	95	2.308 ns	587.5 ps	10.14 ns	9.551 ns	1.785 ns	95
Meas8	tDIPW-Low	Ref1	2.291 ns	244.5 ps	9.929 ns	9.685 ns	1.726 ns	108	2.291 ns	244.5 ps	9.929 ns	9.685 ns	1.726 ns	108
Meas9	SRQse-Fall(DQ)	Ref1	-5.674 V/ns	-9.972 V/ns	-676.0 mV/ns	9.094 V/ns	1.736 V/ns	98	-5.674 V/ns	-9.972 V/ns	-676.0 mV/ns	9.094 V/ns	1.736 V/ns	98
Meas10	SRQse-Rise(DQ)	Ref1	3.483 V/ns	1.059 V/ns	5.052 V/ns	3.993 V/ns	661.1 mV/ns	105	3.483 V/ns	1.059 V/ns	5.052 V/ns	3.993 V/ns	661.1 mV/ns	105
Meas11	VOH(MBIAO)	Ref2	910.7 mV	726.0 mV	980.0 mV	264.0 mV	60.66 mV	220	910.7 mV	726.0 mV	980.0 mV	264.0 mV	60.66 mV	220
Meas12	VOL(MBIAO)	Ref2	-845.9 mV	-942.0 mV	-762.0 mV	180.0 mV	36.86 mV	220	-845.9 mV	-942.0 mV	-762.0 mV	180.0 mV	36.86 mV	220
Meas13	tDQSCK-Dif	Ref3 Ref2	106.3 ps	-1.237 ns	1.227 ns	2.463 ns	712.1 ps	219	106.3 ps	-1.237 ns	1.227 ns	2.463 ns	712.1 ps	219
Meas14	tDQSQ-Dif	Ref1 Ref2	33.10 ps	-452.8 ps	189.2 ps	642.0 ps	119.7 ps	216	33.10 ps	-452.8 ps	189.2 ps	642.0 ps	119.7 ps	216
Meas15	tDVAC(DQS)	Ref2	1.100 ns	0.000 s	1.267 ns	1.267 ns	262.3 ps	464	1.100 ns	0.000 s	1.267 ns	1.267 ns	262.3 ps	464
Meas16	tDH	Ref2 Ref1	1.303 ns	629.5 ps	1.478 ns	848.9 ps	108.0 ps	205	1.303 ns	629.5 ps	1.478 ns	848.9 ps	108.0 ps	205
Meas17	tDSH	Ref2	1.167 ns	301.8 ps	1.351 ns	1.049 ns	268.5 ps	244	1.167 ns	301.8 ps	1.351 ns	1.049 ns	268.5 ps	244
Meas18	tDSL	Ref2	1.230 ns	1.184 ns	1.319 ns	134.9 ps	26.68 ps	220	1.230 ns	1.184 ns	1.319 ns	134.9 ps	26.68 ps	220
Meas19	tRPRE	Ref2	1.085 tCK(avg)	1.045 tCK(avg)	1.097 tCK(avg)	51.32 mtCK(avg)	11.04 mtCK(avg)	24	1.085 tCK(avg)	1.045 tCK(avg)	1.097 tCK(avg)	51.32 mtCK(avg)	11.04 mtCK(avg)	24
Meas20	tRPST	Ref2	286.9 mtCK(avg)	151.3 mtCK(avg)	447.0 mtCK(avg)	295.7 mtCK(avg)	131.6 mtCK(avg)	24	286.9 mtCK(avg)	151.3 mtCK(avg)	447.0 mtCK(avg)	295.7 mtCK(avg)	131.6 mtCK(avg)	24
Meas21	SRQdS-Fall(DQS)	Ref2	-9.570 V/ns	-11.90 V/ns	-980.9 mV/ns	10.14 V/ns	780.4 mV/ns	221	-9.570 V/ns	-11.90 V/ns	-980.9 mV/ns	10.14 V/ns	780.4 mV/ns	221
Meas22	SRQdS-Rise(DQS)	Ref2	7.746 V/ns	2.424 V/ns	9.208 V/ns	6.784 V/ns	1.398 V/ns	221	7.746 V/ns	2.424 V/ns	9.208 V/ns	6.784 V/ns	1.398 V/ns	221

Views

Time Domain View

Page 1 of 5

6-DBDDR3 test report. Saved manually after debugging DDR designs on the 6 Series MSO

DDRA vs 6-CMDDR3 Feature Comparison

Features	DDRA (DPO/MSO 70k)	DDR3 Debug (DBDDR3)	DDR3 Automation (CMDDR3)
Persona	Design Engineer	Design Engineer	Design, Validation, Characterization
DDR3/LPDDR3 Analog Measurement Coverage	100%	100% (DDR3 Unique Measurements) ; Base Measurements using setup files	100% (DDR3 Unique + Base Measurements)
Digital Measurements Support	Yes; only on MSO scope	Yes	Yes
Debug vs Automated Testing	Debug and Semi Automated (DPOJET)	Debug Only	Debug and Fully Automated
Inputs Supported	Analog and MSO (Digital) channels	Analog and MSO (Digital) channels	Analog and MSO (Digital) channels
Visual Trigger (VT)	Yes	Yes	Yes
Limits Capability	Yes (Pass/Fail result in report)	No (All tests are informative; limits in MOI)	Yes
Burst Detection Method	1. DQ+DQS Phase Alignment 2. DQ+DQS Phase Alignment + CS 3. Logic Probe + Latency	1. DQ+DQS Phase Alignment	1. DQ+DQS Phase Alignment 2. DQ+DQS Phase Alignment + CS 3. Logic Probe + Latency
Probing Mechanism	P77XX series + flex tips P75XX series, P6780 Logic probes	TDP77XX series + flex tips TLP058 Logic Probes	TDP77XX series + flex tips TLP058 Logic Probes
De-embedding Support	Yes; using SDLA	Yes; Manually using MATH subsystem	Yes; bundle static .flt files with Compliance SW.
Reporting	Basic – Setup and Results with Pass/Fail	Basic - Setup and Results	Advanced – Results with screenshots

Ordering Information

- Oscilloscope
  - 6 Series MSO with a recommended bandwidth of 8GHz (Opt. 6-BW-8000);
- Probes
  - 3x TDP7708 with P77STFLXB tips (DQ, DQS and Clock signal access)
  - 1x TLP058 (if the DUT supports Digital Channels)
- Software Options
  - Opt. 6-CMDDR3 – DDR3 and LPDDR3 Automated Compliance Solution
  - Opt. 6-DBDDR3 – DDR3 and LPDDR3 Analysis and Debug Solution
  - Opt. 6-DJA – For Eye diagram and other detailed waveform analysis
  - Opt. 6-WIN – Windows 10 OS (Required if ordering 6-CMDDR3)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