Fundamentals of Semiconductor C-V Measurements

Lee Stauffer, Keithley Instruments, Inc.

C-V measurements provide a wealth of information about device and material characteristics.

A Universal Test

Capacitance-voltage (C-V) testing is widely used to determine semiconductor parameters, particularly in MOSCAP and MOSFET structures. However, other types of semiconductor devices and technologies can also be characterized with C-V measurements, including bipolar junction transistors (BJTs), JFETs, III-V compound devices, photovoltaic cells, MEMs devices, organic TFT displays, photodiodes, carbon nanotubes (CNTs), and many others.

The fundamental nature of these measurements makes them useful in a wide range of applications and disciplines. They are used in the research labs of universities and semiconductor manufacturers to evaluate new materials, processes, devices, and circuits. C-V measurements are extremely important to product and yield enhancement engineers, who are responsible for improving processes and device performance. Reliability engineers use these measurements to qualify material suppliers, monitor process parameters, and analyze failure mechanisms.

With appropriate methodologies, instrumentation, and software, a multitude of semiconductor device and material parameters can be derived. This information is used all along the production chain beginning with evaluation of epitaxially grown crystals, including parameters such as average doping concentration, doping profiles, and carrier lifetimes. In wafer processes, C-V measurements can reveal oxide thickness, oxide charges, mobile ions (contamination), and interface trap density. These measurements continue to be used after other process steps, such as lithography, etching, cleaning, dielectric and polysilicon depositions, and metallization. After devices are fully fabricated on the wafer, C-V is used to characterize threshold voltages and other parameters during reliability and basic device testing and to model the performance of these devices.

The Physics of Semiconductor Capacitance

A MOSCAP structure is a fundamental device formed during semiconductor fabrication (see *Figure 1*). Although these devices may be used in actual circuits, they are typically integrated into fabrication processes as a test structure. Since they are simple structures and their fabrication is easy to control, they are a convenient way to evaluate the underlying processes.

The metal/polysilicon layer shown in *Figure 1* is one plate of the capacitor, and silicon dioxide is the insulator. Since the substrate below the insulating layer is a semiconducting material, it is not by itself the other plate of the capacitor. In effect, the majority charge carriers become the other plate. Physically, capacitance, *C*, is determined from the variables in the following equation:

$C = A\,(\kappa/d)$, where

A   is the area of the capacitor,

κ is the dielectric constant of the insulator, and

d   is the separation of the two plates.

Therefore, the larger *A* and κ are, and the thinner the insulator is, the higher the capacitance will be. Typically, semiconductor capacitance values range from nanofarads to picofarads, or smaller.

The procedure for taking C-V measurements involves the application of DC bias voltages across the capacitor while making the measurements with an AC signal (*Figure 1*). Commonly, AC frequencies from about 10kHz to 10MHz are used for these measurements. The bias is applied as a DC voltage sweep that drives the MOSCAP structure from its accumulation region into the depletion region, and then into inversion (*Figure 2*).

A strong DC bias causes majority carriers in the substrate to accumulate near the insulator interface. Since they can't get through the insulating layer, capacitance is at a maximum in the accumulation region as
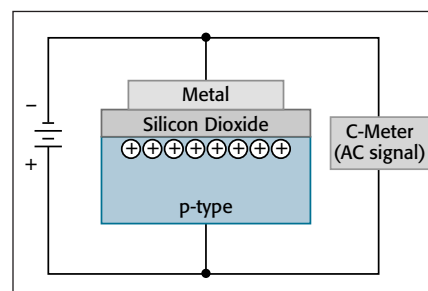

Figure 1. C-V measurement circuit for a MOSCAP structure formed on a P-type substrate.
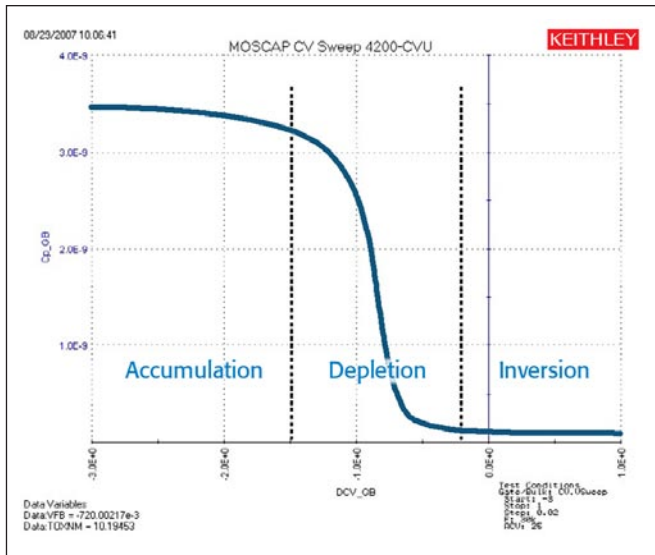
Figure 2. DC bias sweep of MOSCAP structure obtained during C-V testing.

Figure 3. Basic test setup for C-V measurements.

the charges stack up near that interface (i.e., *d* is at a minimum). See *Figure 1*. One of the fundamental parameters that can be derived from C-V accumulation measurements is the silicon dioxide thickness, t_{ox}.

As bias voltage is decreased, majority carriers get pushed away from the oxide interface and the depletion region forms. When the bias voltage is reversed, charge carriers move the greatest distance from the oxide layer, and capacitance is at a minimum (i.e., *d* is at a maximum). From this inversion region capacitance, the number of majority carriers can be derived. The same basic concepts apply to MOSFET transistors, even though their physical structure and doping is more complex.

Many other parameters can be derived from the three regions shown in *Figure 2* as the bias voltage is swept through them. Different AC signal frequencies can reveal additional details. Low frequencies reveal what are called quasistatic characteristics, whereas high frequency testing is more indicative of dynamic performance. Both types of C-V testing are often required.

Basic Test Setup

Figure 3 is the block diagram of a basic C-V measurement setup. Because C-V measurements are actually made at AC frequencies, the capacitance for the device under test (DUT) is calculated with the following:

$C_{DUT} = I_{DUT} / 2\pi f V_{AC}$, where

I_{DUT} is the magnitude of the AC current through the DUT,

f   is the test frequency, and

V_{AC} is the magnitude and phase angle of the measured AC voltage

In other words, the test measures the AC impedance of the DUT by applying an AC voltage and measuring the resulting AC current, AC voltage, and impedance phase angle between them.

These measurements take into account series and parallel resistance associated with the capacitance, as well as the dissipation factor (leakage). *Figure 4* illustrates the basic circuit variables that can be derived from the measurements.
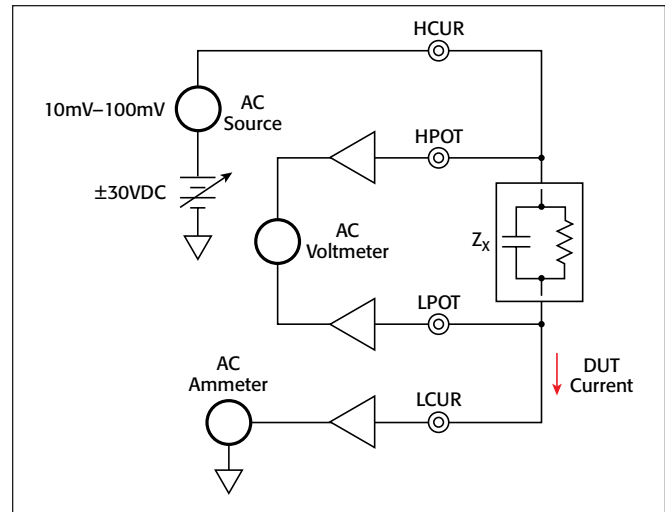
Challenges to Successful C-V Measurements

The block diagram of a C-V test setup (*Figure 3*) is deceptively simple. However, certain challenges are associated with this testing. Typically, test personnel have problems in the following areas:
- Low capacitance measurements (picofarads and smaller values)
- C-V instrument connections (through a prober) to the wafer device
- Leaky (high D) capacitance measurements
- Using hardware and software to acquire the data
- Parameter extractions

Overcoming these challenges requires careful attention to the techniques used along with appropriate hardware and software.

Low Capacitance Measurements. If *C* is small, the DUT's AC response current is small and hard to measure. However, at higher frequencies, the DUT impedance is reduced, so the current increases and is easier to measure. Often semiconductor capacitance is very low (less than 1pF), which is below the capabilities of many LCR meters. Even those claiming to measure these small capacitance values may have confusing specifications that make it difficult to determine the final accuracy in the measurement. If accuracy over the instrument's full measurement range is not explicitly stated, the user needs to clarify this with the manufacturer.

High D (Leaky) Capacitors. In addition to having a low *C* value, a semiconductor capacitor may also be leaky. That is the case when the equivalent R in parallel with *C* is too low. This results in resistive impedance overwhelming the capacitive impedance, and the *C* value gets lost in the noise. For devices with ultra-thin oxide layers, *D* values can be greater than five. In general, as *D* increases, the accuracy of a *C* measurement is rapidly degraded, so high *D* is a limiting factor in the practical use of a C meter. Again, higher frequencies can help solve the problem. At higher frequencies the capacitive impedance is lower, resulting in a *C* current that is higher and more easily measured.

C-V Measurement Connections. In most test environments, the DUT is a test structure on a wafer: It is connected to the C-V instrument through a prober, a probe card adapter, and a switch matrix. Even if no switch is involved, there is still a prober and significant
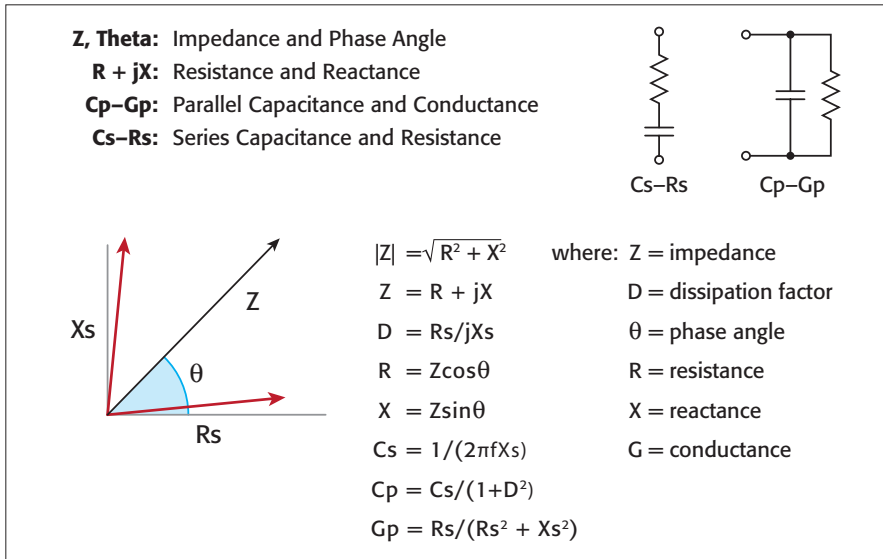
Z, Theta: Impedance and Phase Angle
R + jX: Resistance and Reactance
Cp–Gp: Parallel Capacitance and Conductance
Cs–Rs: Series Capacitance and Resistance

Cs–Rs   Cp–Gp

$$|Z| = \sqrt{R^2 + X^2}$$

where:
Z = impedance
$Z = R + jX$
D = dissipation factor
$D = Rs/jXs$
θ = phase angle
$R = Z\cos\theta$
R = resistance
$X = Z\sin\theta$
X = reactance
$Cs = 1/(2\pi fXs)$
G = conductance
$Cp = Cs/(1+D^2)$
$Gp = Rs/(Rs^2 + Xs^2)$

Figure 4. Basic electrical variables available from C-V measurements.

cabling. At high frequencies, special corrections and compensation must be applied. Usually, this is achieved with some combination of an open, short, or calibration device. Because of the complexity of the hardware, cabling, and compensation techniques, it is a good idea to confer with C-V test application engineers. They are skilled at working with various probe systems to overcome many types of interconnection problems.

Obtaining Useful Data. In addition to the accuracy issues mentioned earlier, practical considerations in C-V data collection include the instrumentation's range of test variables, versatility of parameter extraction software, and ease of hardware usage. Traditionally, C-V testing has been limited to about 30V and 10mA DC bias. However, many applications, such as characterizing LD MOS structures, low-κ interlayer dielectrics,

MEMs devices, organic TFT displays, and photodiodes, require tests at higher voltage or current. For these applications, a separate high voltage DC power supply and C meter are required; DC bias up to 400V differential (0 to ±400V) and a current output up to 300mA are very useful. Being able to apply differential DC bias on both the HI and LO terminals of the C-V instrument offers more flexible control over electric fields within the DUT, which is very helpful in the research and modeling of novel devices, such as nanoscale components.

The instrumentation software should include ready-to-run test routines that do not require user programming. These should be available for the most widely used device technologies and test regimens, which were mentioned in the first three paragraphs of this article. Some researchers may also be

interested in less common tests, such as performing both a C-V and C-f sweep on a Metal-Insulator-Metal (MIM) capacitor, measuring small interconnect capacitance on a wafer, or doing a C-V sweep on a two-terminal nanowire device. The parameter extractions should be easily obtained, with automated curve plotting. (See, for example, *Figure 5*.)

Often, engineers and researchers are expected to perform C-V measurements with little experience and training on the instrumentation. A test system with an intuitive user interface and easy-to-use features makes this practical. That includes simple test setup, sequence control, and data analysis. Otherwise, the user spends more time learning the system than collecting and using the data. Other considerations are a test system with:

- Tightly integrated source-measure units, digital oscilloscope and C-V meter
- Easy integration with other external instruments
- High resolution and precise measurements at the probe tips (DC biasing down to millivolts and capacitance measurements down to femtofarads)
- Test setups and libraries that can be easily modified
- Diagnostic/troubleshooting tools that let users know whether or not the system is performing correctly. KEITHLEY
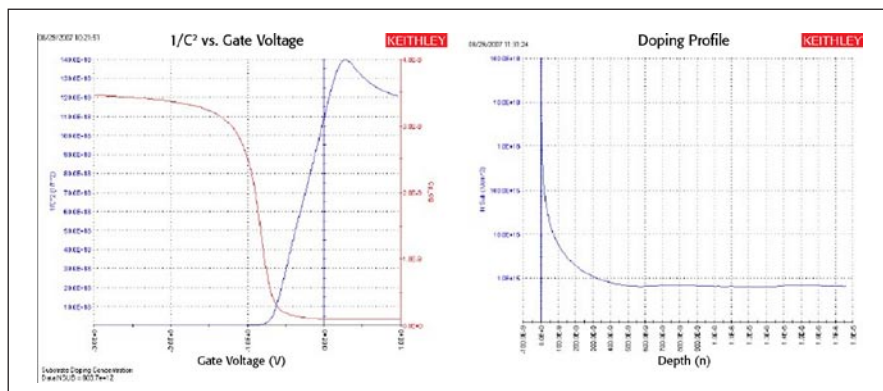

Figure 5. Example of parameter extractions from a Keithley Model 4200-SCS showing doping characteristics (blue curve on left), which is related to the reciprocal of 1/C² vs. Vg (red curve). The right graph shows the doping profile as the number of carriers per cubic centimeter as a function of substrate depth.

About the Author

Lee Stauffer is a Senior Marketer with Keithley Instruments in Cleveland, Ohio, USA, where he is responsible for developing and supporting products for the semiconductor manufacturing and research markets. His formal education in electrical engineering and semiconductor device physics is complemented by 20 years experience in semiconductor process and product engineering, device characterization, and instrumentation design. He can be reached at 440-248-0400, or by e-mail at lstauffer@keithley.com.

KEITHLEY

A G R E A T E R M E A S U R E O F C O N F I D E N C E

KEITHLEY INSTRUMENTS, INC. ■ 28775 AURORA ROAD ■ CLEVELAND, OHIO 44139-1891 ■ 440-248-0400 ■ Fax: 440-248-6168 ■ 1-888-KEITHLEY ■ www.keithley.com

BELGIUM
Sint-Pieters-Leeuw
Ph: 02-3630040
Fax: 02-3630064
info@keithley.nl
www.keithley.nl

CHINA
Beijing
Ph: 8610-82255010
Fax: 8610-82255018
china@keithley.com
www.keithley.com.cn

FINLAND
Espoo
Ph: 09-88171661
Fax: 09-88171662
finland@keithley.com
www.keithley.com

FRANCE
Saint-Aubin
Ph: 01-64532020
Fax: 01-60117726
info@keithley.fr
www.keithley.fr

GERMANY
Germering
Ph: 089-84930740
Fax: 089-84930734
info@keithley.de
www.keithley.de

INDIA
Bangalore
Ph: 080-26771071, -72, -73
Fax: 080-26771076
support_india@keithley.com
www.keithley.com

ITALY
Peschiera Borromeo (Mi)
Ph: 02-5538421
Fax: 02-55384228
info@keithley.it
www.keithley.it

JAPAN
Tokyo
Ph: 81-3-5733-7555
Fax: 81-3-5733-7556
info.jp@keithley.com
www.keithley.jp

KOREA
Seoul
Ph: 82-2-574-7778
Fax: 82-2-574-7838
keithley@keithley.co.kr
www.keithley.co.kr

MALAYSIA
Penang
Ph: 60-4-643-9679
Fax: 60-4-643-3794
chan_patrick@keithley.com
www.keithley.com

NETHERLANDS
Gorinchem
Ph: 0183-635333
Fax: 0183-630821
info@keithley.nl
www.keithley.nl

SINGAPORE
Singapore
Ph: 65-6747-9077
Fax: 65-6747-2991
koh_william@keithley.com
www.keithley.com.sg

SWEDEN
Stenungsund
Ph: 08-50904600
Fax: 08-6552610
sweden@keithley.com
www.keithley.com

SWITZERLAND
Zürich
Ph: 044-8219444
Fax: 044-8203081
info@keithley.ch
www.keithley.ch

TAIWAN
Hsinchu
Ph: 886-3-572-9077
Fax: 886-3-572-9031
info_tw@keithley.com
www.keithley.com.tw

UNITED KINGDOM
Theale
Ph: 0118-9297500
Fax: 0118-9297519
info@keithley.co.uk
www.keithley.co.uk

© Copyright 2009 Keithley Instruments, Inc.   Printed in the U.S.A.   No. 3019   02.04.09