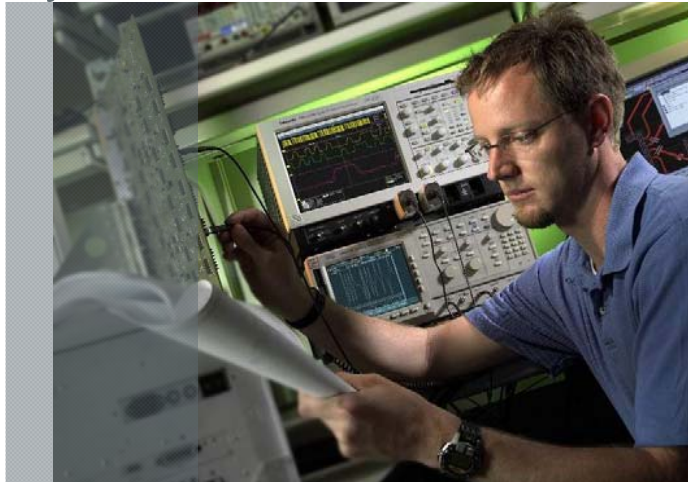


MIPI technology and Tek test solution



Oct. 25th 2011
Ryan Yu



Tektronix[®]

Agenda

- MIPI Standards Overview
- MIPI PHY Testing (D-PHY and M-PHY)
- MIPI CSI/DSI/DigRF
- Summary, Q&A

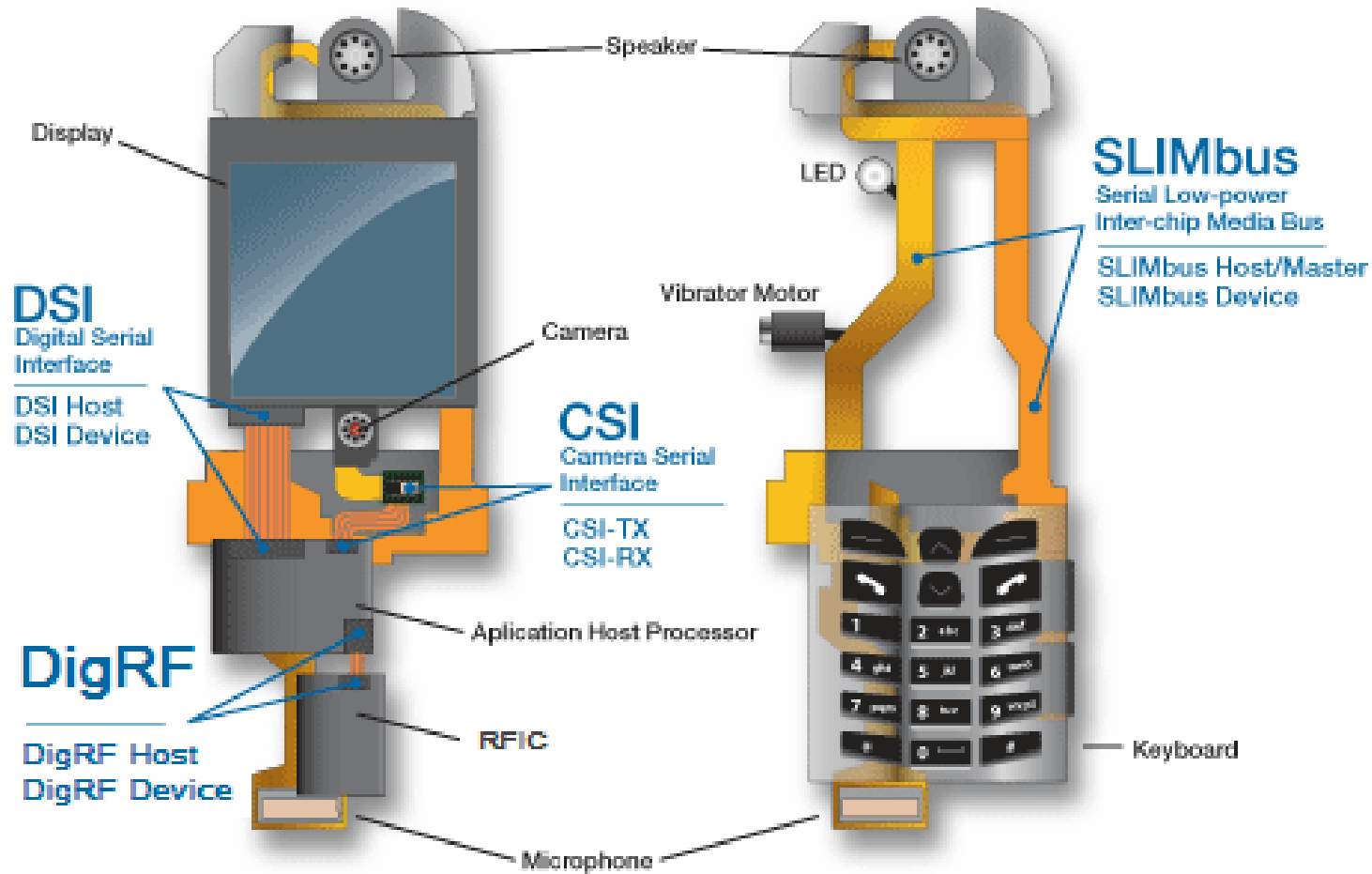


Tektronix & MIPI Alliance

- Tektronix is a **Contributor Member** of the MIPI Alliance
 - Tektronix participates in several MIPI Working Groups.
- Tektronix Testing Support for MIPI includes;
 - Analog Validation
 - Protocol Debug and Verification
- Tektronix is engaged on MIPI Test Methodologies working alongside the UNH-IOL.

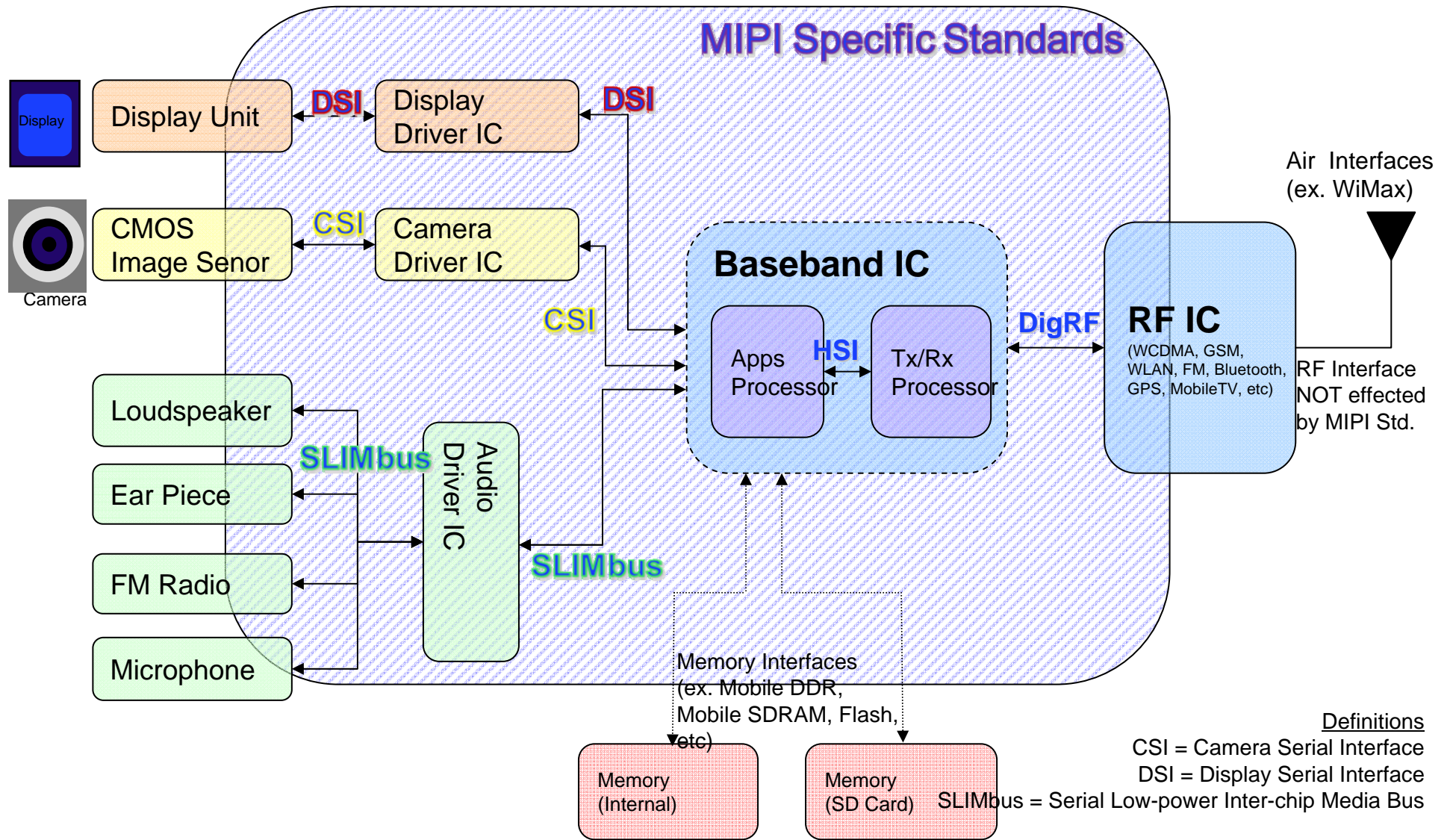


Example of Mobile Terminal



MIPI Standards Overview

Example Mobile Terminal Block Diagram



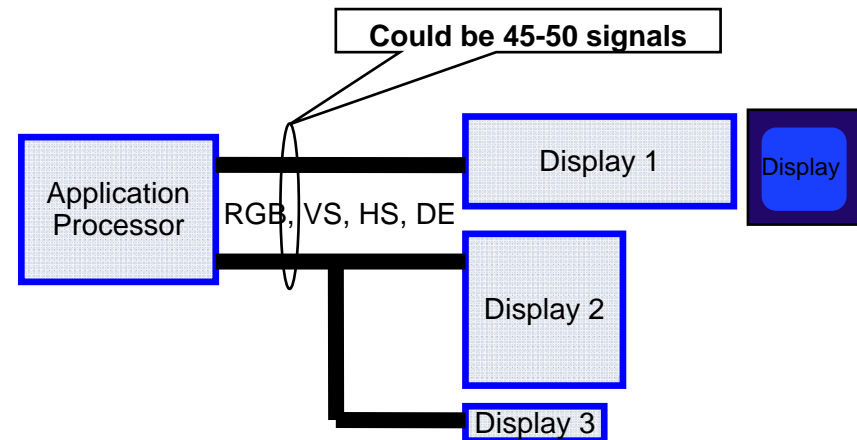
Definitions
 CSI = Camera Serial Interface
 DSI = Display Serial Interface
 SLIMbus = Serial Low-power Inter-chip Media Bus

What is MIPI DSI ?

- DSI is the specification for processor-to-display interconnect in handheld platforms

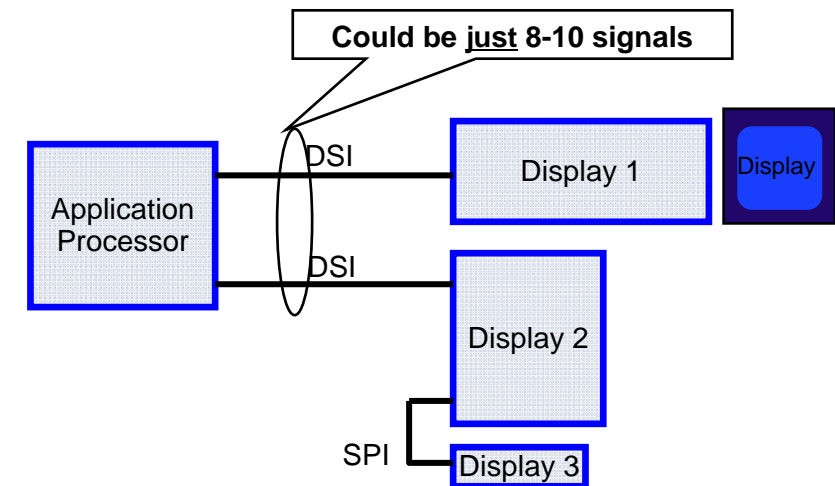
- Legacy Standards in a Mobile Device**

- Exposed wide standards
 - RGB, VS, HS, DE
- All are parallel busses
 - Each 45-50 signals



- MIPI DSI-1**

- Physical layer is D-Phy
- Protocol layer is DSI-1
- Only Single standard: DSI-1
 - Multiple Displays – One Interface
 - Supports all Common Display technologies
- A Serial bus
 - Just 8-10 signals
 - 5:1 ratio savings in signals
 - Lower EMI



- MIPI DSI-2**

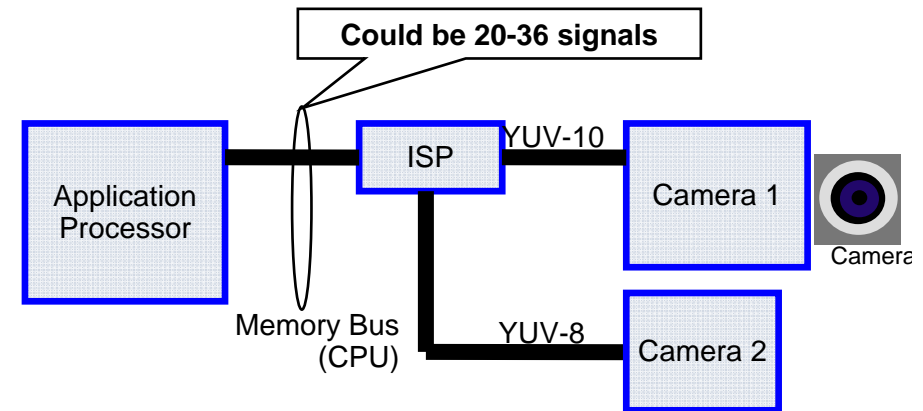
- Physical layer is M-Phy
- Protocol layer is DSI-2
- Higher Datarate
 - Backward Compatible to DSI

What is MIPI CSI ?

- CSI is the serial interface specification for Camera/ imaging peripherals and host processors

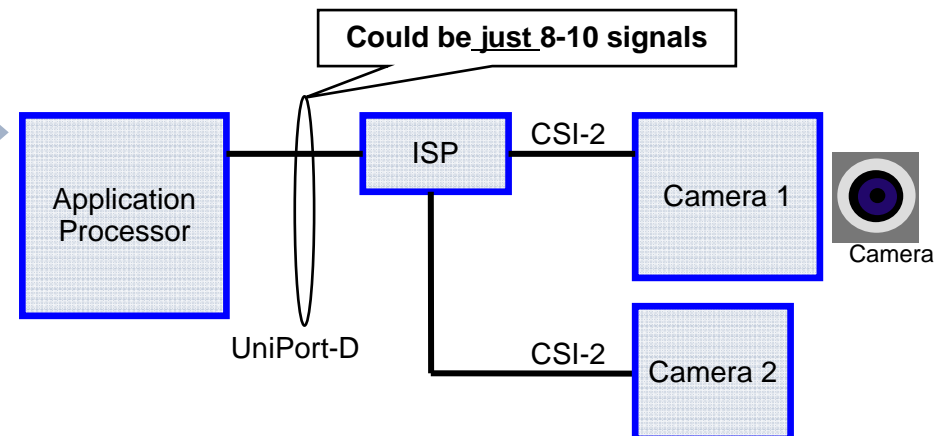
- The Legacy Standards in a Mobile Device

- Exposed wide standards
 - YUV-10, YUV-8, etc
- All are parallel busses
 - Each 20-36 signals



- MIPI CSI-2

- Physical layer is D-Phy
- Protocol layer is CSI-2
- Only Single standard
 - Multiple Cameras – One Interface
- A Serial bus
 - Just 8-10 signals
 - 3:1 ratio savings in signals
 - Lower EMI

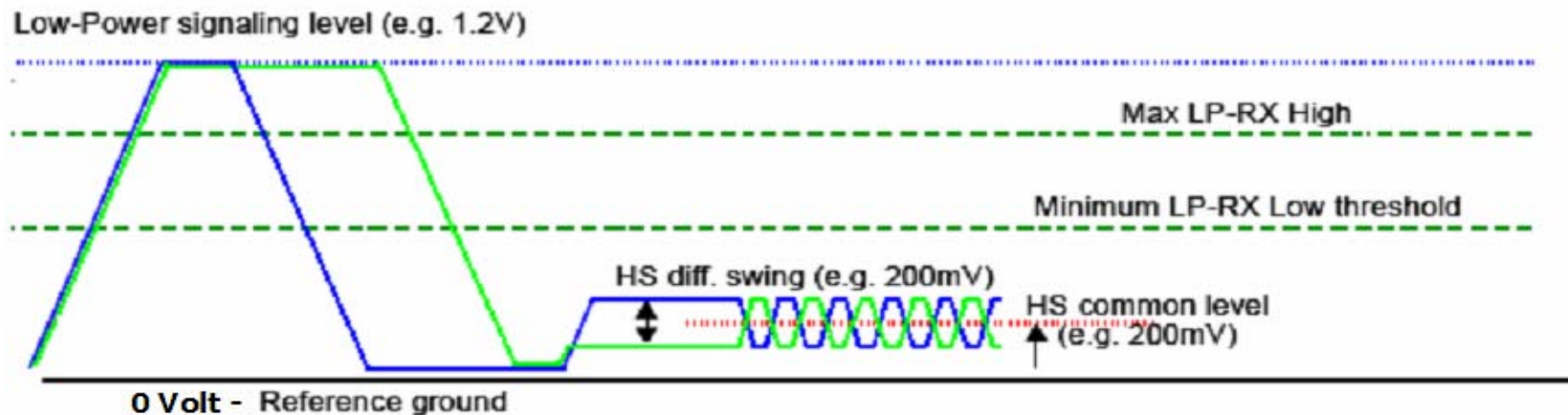


- MIPI CSI-3

- Physical layer is M-Phy
- Protocol layer is CSI-3
- Higher Datarate
 - Backward Compatible to CSI-2

What is MIPI D-PHY ?

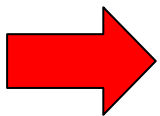
- It's a PHY standard for interfacing Camera (CSI) & Display (DSI)
- Two modes of transmission
 - High Speed (HS) and Low Power (LP)
- Modes are mixed during the operation
 - Transitions from LP to HS and back to LP on the fly
- Maximum Data Rate
 - High Speed mode: 80 Mbps – 1 Gbps, Typically at ~500 Mbps.
 - Low Power mode: Up to 10 Mbps
- Bus termination
 - 50 ohms in HS
 - Hi-Z in LP
- Dual simplex communication. Bi-directional & Half-duplex are optional.





D-PHY Testing Challenges

- Logo/Compliance testing is NOT required, but Optional.
 - MIPI is Chip-to-Chip/ Chip-to-Peripheral interface, **similar to DDR.**
 - Mobile Phones do NOT need compliance logos, **unlike USB/ SATA**
- Bursty, High/Low amplitude nature of D-PHY Tx signaling behavior makes measurement setups critical for proper evaluation
 - Vertical scaling
 - High-Impedance probing
 - Sample rate
- Characterization is significantly important
 - Mobile OEMs select the suppliers based on characterization reports.
- No two MIPI devices are the same
 - Specification enables **custom limits.**
 - Up to 4 lanes of Data traffic, Variable Data Rates
 - Multiple different data formats



Test Equipment & Setups need to be Very Flexible

MIPI Alliance D-PHY CTS and Tektronix



MIPI Alliance Testing Program

Version 1.00
30-August 2010

MIPI Alliance Testing Program User's Manual, Method of Implementation (MOI), and Tutorial Documentation for D-PHY Physical Layer Transmitter Conformance Tests, Using Agilent, LeCroy, and Tektronix Real-Time DSOs, and DPHYGUI TX Conformance Software (v20100830)

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D-PHY Tx Testing Solution – Continued

■ Scope

- **Recommend: DPO7354 or DPO/DSA/MSO70404/B**
 - For risetime (150ps) measurements within +/-5% of spec
- DPO7254 can be used when risetime is **NOT** a concern.

■ Probes

– Probing Considerations

- Measure both SE and Diff performance
- Must have >1.2V dynamic range
- Needs minimum probe attenuation
 - 1X best, but 2.5X or 5X ok

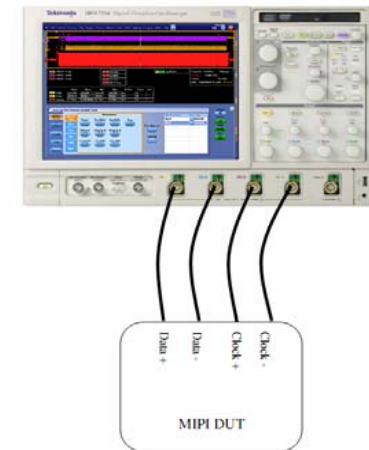
– Recommend:

- **Four TAP3500 for DPO7000 or Four P7240 for MSO/DPO/DSA70000/B**
- (Ch1: D+), (Ch2: D-), (Ch3: Clk+), (Ch4: Clk-)
- TAP2500 fine for low datarate DUTs

– Alternatives:

– For Solder-Down

- **TDP3500 for DPO7000 or P73xx for 70000 Series**
- (Ch1: D+, Gnd), (Ch2: D-, Gnd), (Ch3: Clk+ & Clk-)



D-PHY Tx Testing Solution from Tektronix

- New Tektronix Oscilloscope Option; MIPI D-PHY Essentials
 - An option to DPOJET Analysis providing specific D-PHY setup library & MOI
 - Automated measurement set
 - Based on D-PHY Base Spec v0.9 and UNH's Conformance Test Suite v0.08.
 - Compatible with Tektronix DPO7000, DPO/DSA70000/B and MSO70000 oscilloscopes
- Requires DPOJET Advanced Timing & Analysis Software
- Benefits
 - Characterization
 - Proper vertical settings
 - Breadth of Tests Coverage
 - Comprehensive Test Reports



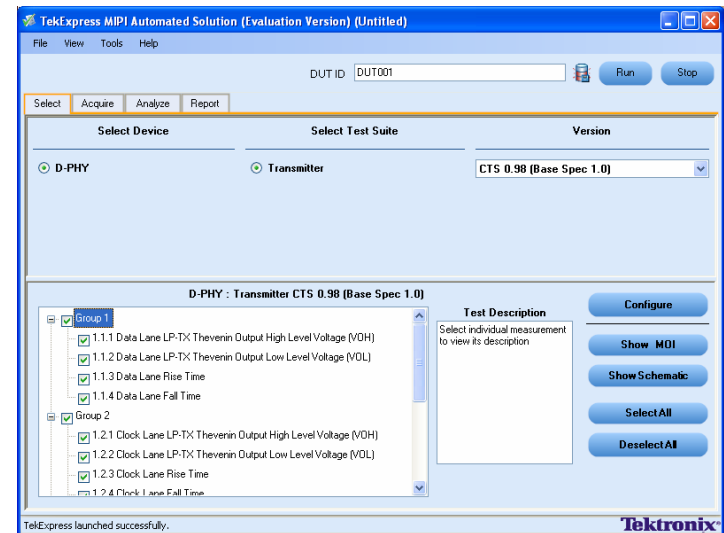
Opt.D-PHY (*Existing*)

- Opt.D-PHY : D-PHY Essentials
 - DPOJET option for setup library &MOI
 - Automation similar to Opt. USB3 or Opt. PCE
 - Provides Debug Analysis and Characterization Testing
 - Based on D-PHY Base Spec v0.9 and UNH's Conformance Test Suite v0.08.
 - Runs on DPO7000, DPO/DSA/MSO70000/B Series oscilloscopes
- Opt.DJA is Pre-Requisite
- Differentiation
 - Flexible for Debug Analysis &Characterization
 - Breadth of Tests Coverage
- Value proposition
 - DPOJET Detailed Test Reports
 - DPOJET Scalable for early start on M-PHY (Next Generation Standard)
 - Tek 3.5GHz scope is the minimal configuration for accurate testing
 - i.e. unlike Agilent 4G scope at entry-level



New Opt.D-PHYTX

- Opt.D-PHYTX : D-PHY Automated Solution
 - TekExpress option for Fully-Automated testing
 - Automation similar to Opt.USB-TX
 - Provides Conformance and Characterization Testing
 - Based on D-PHY Base Spec v1.0 and UNH's Conformance Test Suite v0.98.
 - Runs on DPO7000, DPO/DSA/MSO70000/B Series oscilloscopes
- Opt.TEKEXP is Pre-Requisite
- Differentiation
 - Un-parallel Automation (Auto-Cursors/ Regions)
 - For Conformance testing to Latest CTS (v0.98)
 - Based on Latest Base spec (v1.0)
- Value proposition
 - Custom-limits/ Limits-Editing on the fly
 - Test Reports
 - Zoom-in waveform captures at the Cursors/ Regions
 - Pass/Fail Summary with Margin details
 - Tek 3.5GHz scope is the minimal configuration for accurate testing
 - i.e. unlike Agilent 4G scope at entry-level

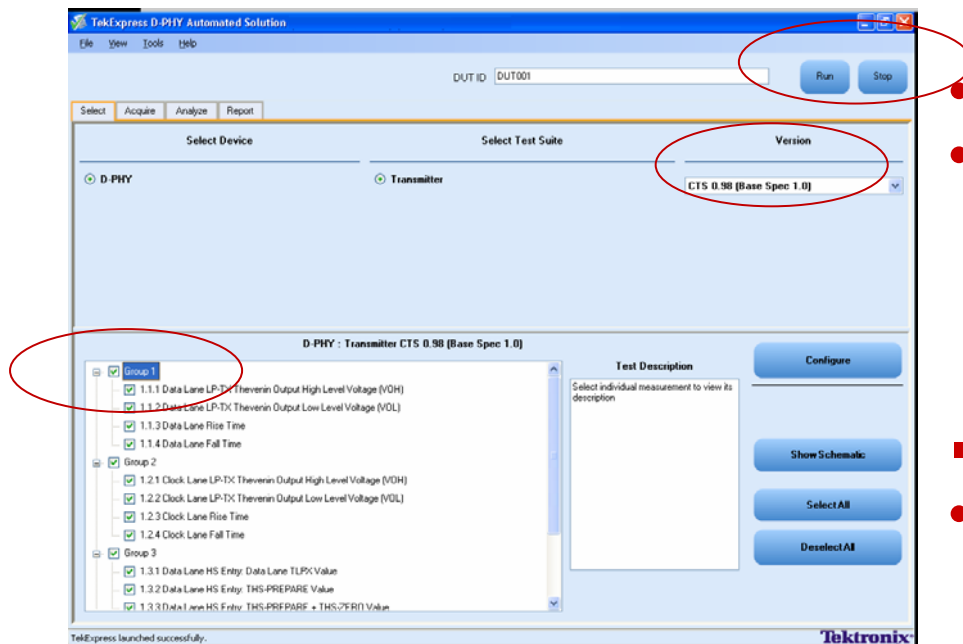


Opt.D-PHYTX and Opt.D-PHY

Testing Recommendations

Feature	Opt.D-PHY (D-PHY Essentials)	Opt.D-PHYTX (D-PHY Automated Solution)
Pre-Requisite tools	DPOJET	TEKEXP
Automatic measurement selections based on device ID, test group, and selected probes.		✓
Single button execution for all measurements		✓
Configurable setup and Editing of test limits	✓	✓
Detailed or Summary Reports	Detailed Only	Detailed &Summary
Automatically Save Test Reports and Waveforms		✓
Re-analyze pre-recorded waveforms	✓	✓
D-PHY Specific User Interface		✓
Base Specification Revision	V0.9	V1.0
Conformance Test Specification Revision	V0.08	V0.98
Testing Recommendation	Debug , Analysis &Characterization	Conformance, Verification, &Characterization

D-PHYTX Select Panel

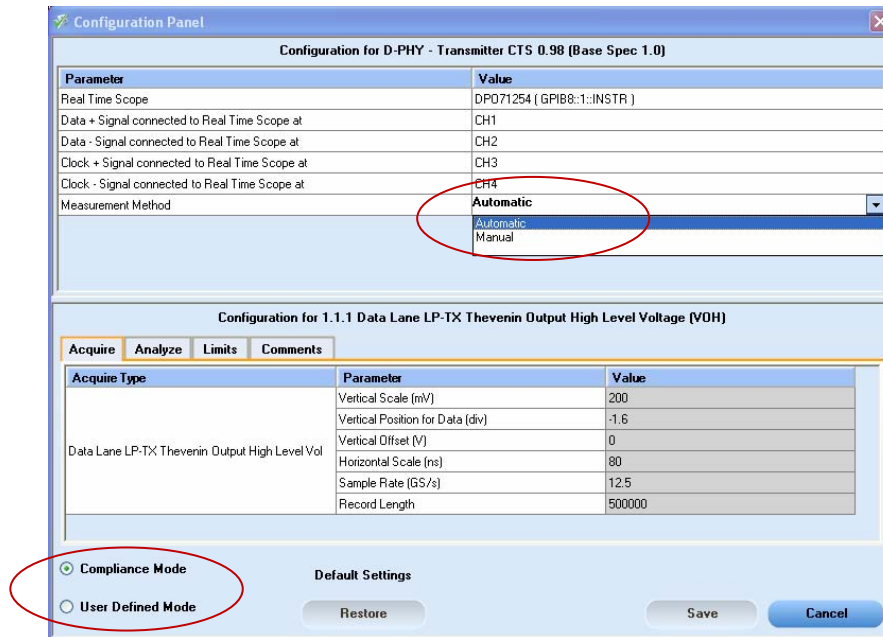


- Feature: Single-Button Testing
 - Perform Single-button Fully-Automated testing

- Feature: Latest CTS
- Benefits:
 - Allows conformance testing to the latest CTS as of date.

- Feature: Selective Testing
- Benefits:
 - Allows selecting individual tests or group-wise tests through tree-structure.

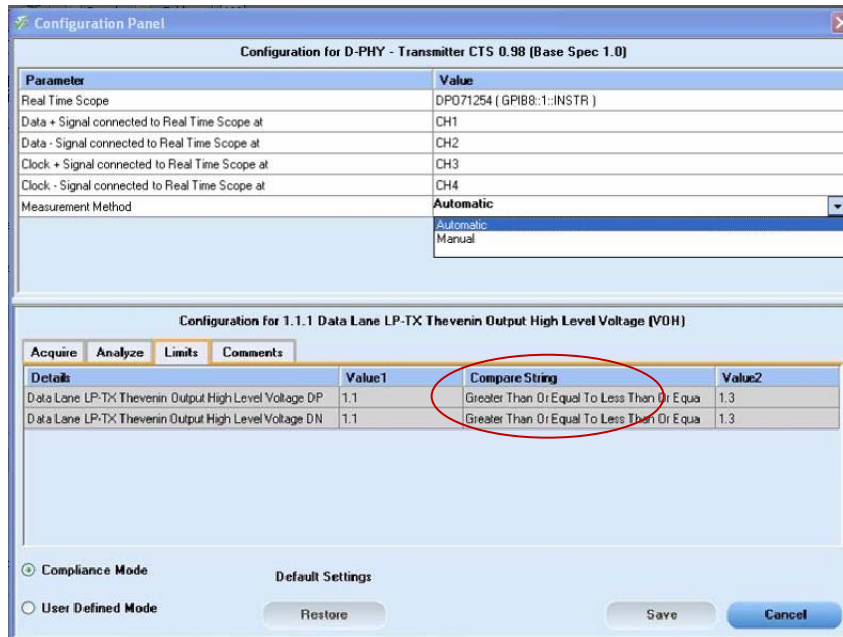
D-PHYTX Configure Panel



- Feature: Automated Testing
- Benefits:
 - Does not require operator intervention to conduct time consuming testing
 - Reduces the amount of time required to conduct testing
 - Enables customers to test devices faster

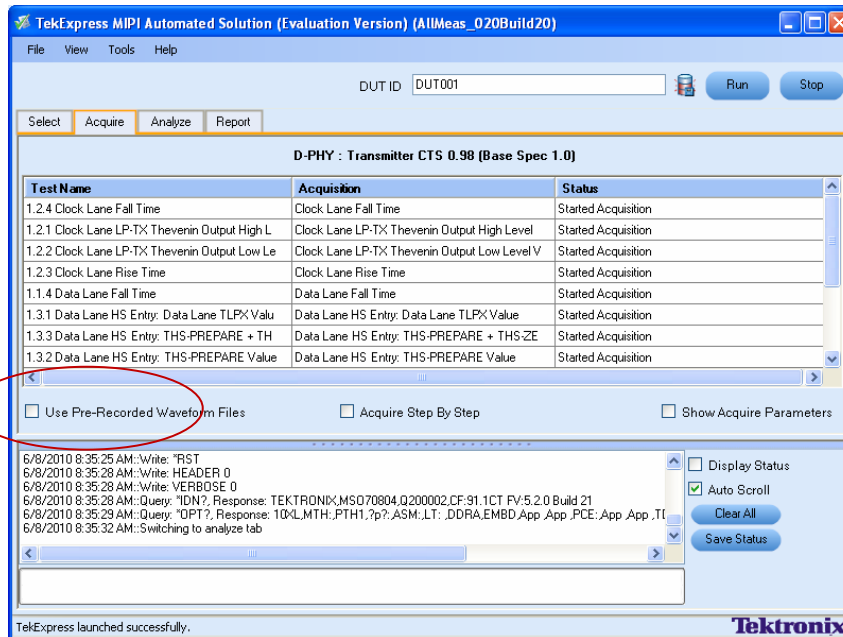
- Feature: Setup Customization/ User-Defined Mode
- Benefits:
 - Modify the test setup as per the DUT configuration.
 - Unit Intervals are automatically calculated based on the DUT datarates.

D-PHYTX Configure Limits Panel



- Feature: Margin Testing/ Characterization
- Benefits:
 - Allows custom-limits or limits-editing to perform Margin testing.
 - Performs characterization of your design.

D-PHYTX Acquire Panel



- Feature: Pre-recorded waveforms
- Benefits:
 - Performs Live or Off-line Analysis through any Windows PC/ system
- Feature: LAN/ GPIB Connectivity
- Benefits:
 - Allows remote execution of tests

D-PHYTX Analyze Panel

6/8/2010 8:55:37 AM: Writing results for 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit
6/8/2010 8:55:37 AM: Inserting images and hyperlinks
6/8/2010 8:55:51 AM: Saving report as MHT in X:\MIPIN\Untitled Session\DUT001\20100608_083514\DUT001.mht
6/8/2010 8:55:53 AM: Closing MS-Excel
6/8/2010 8:55:54 AM: Completed report generation for D-PHY Transmitter
6/8/2010 8:55:54 AM: Test execution completed

Test Name	Status	Low Limit	Measured Value	High Limit	Margin	Pass/Fail Status
1.1.1 Data Lane LP-	Completed	1.1 V	1.168 V	1.3 V	0.068 V, 0.132 V	✓ Pass
1.1.2 Data Lane LP-	Completed	-50 mV	8 mV	50 mV	58.42 mV	✓ Pass
1.1.3 Data Lane Ris	Completed	N.A	10.53 nS	25 nS	14.47 nS	✓ Pass
1.1.4 Data Lane Fal	Completed	N.A	9.76 nS	25 nS	15.24 nS	✓ Pass
1.2.1 Clock Lane L	Completed	1.1 V	1.192 V	1.3 V	0.092 V, 0.108 V	✓ Pass

- Feature:
 - Reliable Results
- Benefits:
 - Avoids double testing, through accurate and reliable results from single-run

D-PHYTX Reports Panel

TekExpress Automation Framework
D-PHY Transmitter Signal Characteristics Test Report

DUT ID : DUT001
 Date/Time : 6/8/2010 8:55
 Device Type : D-PHY
 Execution Time : 20 Min
 CTS Version : CTS 0.98 (Base Spec 1.0)
 Overall Compliance Mode : Yes
 Overall Test Result : **Fail**

Scope Model : MS070804
 Scope Serial Number : 0200002
 Scope FW Version : 5.2.0 BUILD.21
 Probe Model : TX
 Probe Serial Number : 104
 TelExpress Version : BPR 0.2.0.26; Framework: 1.3.5.141
 SPC FactoryCalibration : PASS/PASS

Test Name	Measurement Details	Low Limit	Measured value	High Limit	Units	Test Status	Compliance Mode	Analysis Time	Comments
1.1.1 Data Lane LP-TX Themin Output High Level Voltage (VOL)	Data Lane LP-TX Themin Output High Level Voltage DP	>= 1.1	1.177+00	<= 1.3	0.068 V, 0.132	Pass	No	1 Min	
	Data Lane LP-TX Themin Output High Level Voltage DN	>= 1.1	1.185+00	<= 1.3	0.084 V, 0.116	Pass	No	1 Min	
1.1.2 Data Lane LP-TX Themin Output Low Level Voltage (VOL)	Data Lane LP-TX Themin Output Low Level Voltage DP	>= -50	8.00E+00	<= 50	58.42	Pass	Yes	<1 Min	
	Data Lane LP-TX Themin Output Low Level Voltage DN	>= -50	-8.00E+00	<= 50	42.58	Pass	Yes	<1 Min	
1.1.3 Data Lane Rise Time	Data Lane Rise Time DP	-	1.05E+01	< 25	14.47	nS	Pass	Yes	1 Min
	Data Lane Rise Time DN	-	1.05E+01	< 25	14.5	nS	Pass	Yes	1 Min
1.1.4 Data Lane Fall Time	Data Lane Fall Time DP	-	1.04E+01	< 25	14.65	nS	Pass	Yes	<1 Min
	Data Lane Fall Time DN	-	9.76E+00	< 25	15.24	nS	Pass	Yes	<1 Min
1.2.1 Clock Lane LP-TX Themin Output High Level Voltage (VOL)	Clock Lane LP-TX Themin Output High Level Voltage DP	>= 1.1	1.20E+00	<= 1.3	0.1 V, 0.1	mV	Pass	Yes	1 Min
	Clock Lane LP-TX Themin Output High Level Voltage DN	>= 1.1	1.19E+00	<= 1.3	0.092 V, 0.108	mV	Pass	Yes	1 Min
1.2.2 Clock Lane LP-TX Themin Output Low Level Voltage (VOL)	Clock Lane LP-TX Themin Output Low Level Voltage DP	>= -50	8.00E+00	<= 50	58.42	mV	Pass	Yes	<1 Min
	Clock Lane LP-TX Themin Output Low Level Voltage DN	>= -50	-8.00E+01	<= 50	2.98	mV	Pass	Yes	<1 Min
4.3.3 Clock Lane Rise Time	Clock Lane Rise Time DP	-	4.64E+00	< 25	20.36	nS	Pass

- Feature: Detailed test reports

- Benefits:

- Provides Pass/Fail summary table
- Provides margin details on each test
- Provides waveform screenshot of testing region, through hyperlinks for each test.
- Provides “single-printable” consolidated report for all lanes and all tests.

Opt.D-PHYTX UI-design and Reports

- Clock Continuous mode
- Escape mode

Tektronix
Enabling Innovation

TekExpress Automation Framework
D-PHY Transmitter Signal Characteristics Test Report

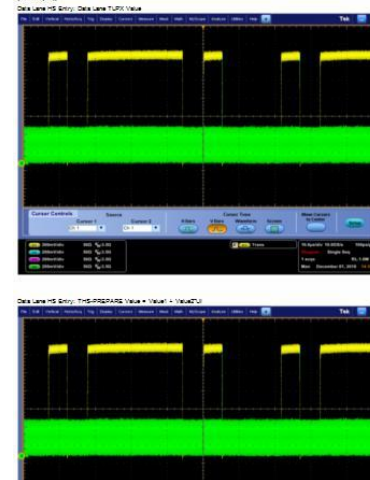
Unit ID: DUT001
Date/Time: 12/22/2016 14:52

Device Type: D-PHY
Execution Time: 23.506

CTS Version: CTS 0.98 (Base Spec 1.0)
Overall Compliance Mode: Pass
Overall Test Result: Pass

Scope Name: DUT001 Scope Serial Number: 000000 Scope File Version: 2.1.1.0.0.0 SPC Factory Calibration: 73887088
 Ch1 Probe Model: ZUP500 Ch1 Probe Serial Number: 000000
 Ch2 Probe Model: ZUP500 Ch2 Probe Serial Number: 000000
 Ch3 Probe Model: ZUP500 Ch3 Probe Serial Number: 000000
 Ch4 Probe Model: ZUP500 Ch4 Probe Serial Number: 000000

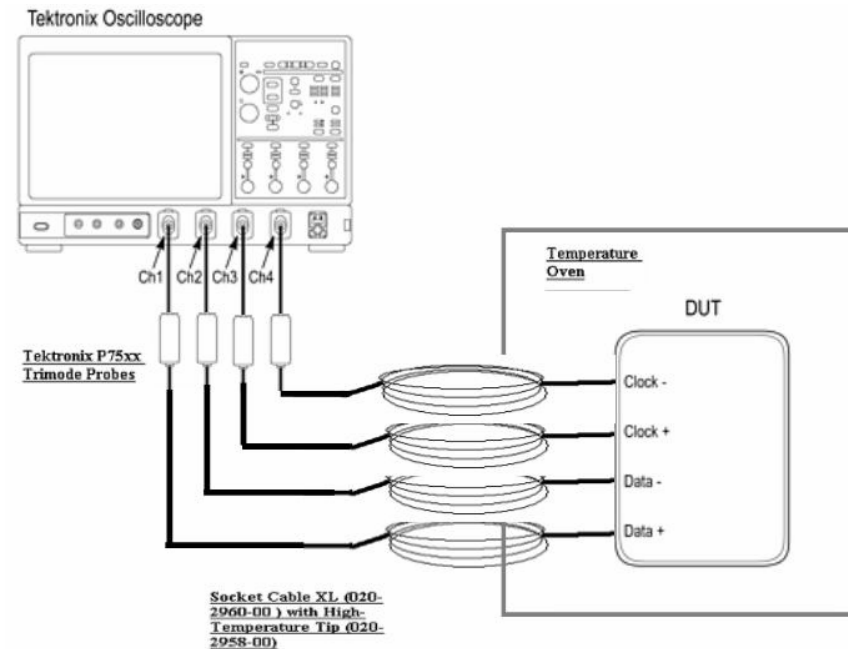
Test Name	Measurement	Unit	Low Limit	Measured Value	High Limit	Margin	Units	Fail	Compliance Mode	Analysis Time	Comments
1.3.1 Data Lane HS Entry: Data Lane TLPX Value	Data Lane HS Entry: Data Lane TLPX Value		++ 40	45.9000000000	-	-4.24	mS	Fail	Yes	1.00s	
1.3.2 Data Lane HS Entry: THS-PREPARE Value	Data Lane HS Entry: THS-PREPARE Value		++ 40	45.8000000000	++ 40	0.84	mS	Pass	Yes	+1.00s	
1.3.3 Data Lane HS Entry: THS-PREPARE + THS-ZERO Value	Data Lane HS Entry: THS-PREPARE + THS-ZERO Value		++ 140	408.4000000000	-	421.40	mS	Pass	Yes	1.00s	
1.3.4 Data Lane HS-TX Differential Voltage (VDD(0), VDD(1))	Data Lane HS-TX Differential Voltage (VDD(0), VDD(1))		++ 140	305.1000000000	++ 270	0.2992	mV	Pass	Yes	+1.00s	
1.3.5 Data Lane HS-TX Differential Voltage Mismatch (VDD)	VDD		-	13.0000000000	+ 10	-0.0000	mV	Fail	Yes	+1.00s	
1.3.6 Data Lane HS-TX Single-Ended Output High Voltages (VDHHS(DP), VDDH(SDP), VDDH(SDU))	Data Lane HS-TX Single-Ended Output High Voltage (VDHHS(DP))		-	477.0000000000	++ 200	-45	mV	Fail	Yes	1.00s	
1.3.7 Data Lane HS-TX Static Common-Mode Voltages (VCMTX(1), VCMTX(2))	Data Lane HS-TX Static Common-Mode Voltage (VCMTX(1))		++ 140	211.8000000000	++ 200	0.0001	mV	Pass	Yes	+1.00s	
1.3.8 Data Lane HS-TX Static Common-Mode Voltage Mismatch (VCMTX(0))	Data Lane HS-TX Static Common-Mode Voltage Mismatch (VCMTX(0))		++ 4	-0.0000000000	++ 5	-2.4878	mV	Pass	Yes	1.00s	
1.3.9 Data Lane HS-TX 20%-20% Rise Time (RT)	Data Lane RT		++ 100	153.7414000000	++	1.7415	ns	Pass	Yes	+1.00s	
1.3.10 Data Lane HS-TX 20%-20% Fall Time (FT)	Data Lane FT		++ 100	141.4021140000	++	0.7415	ns	Fail	Yes	+1.00s	
1.4.1 Data Lane HS Clock Inharmonicity (CLOCK)	VDDHHS(DP)		-	3.4112140000	+ 10.0	-3.4112	mV	Pass	Yes	+1.00s	UI (RT 20% Value) Limit(1) 25
1.4.2 Data Lane HS-TX Dynamic Common-Level Variations Between 50-450mV (VDD(0), VDD(1))	Data Lane HS-TX Dynamic Common-Level Variations (VDD(0), VDD(1))		-	24.4100000000	+ 25	-0.0046	mV	Pass	Yes	1.00s	
1.4.10 Data Lane HS-TX Dynamic Common-Level Variations Above 450mV (VDD(0), VDD(1))	Data Lane HS-TX Dynamic Common-Level Variations (VDD(0), VDD(1))		-	12.7870000000	+ 15	-2.0072	mV	Pass	Yes	1.00s	



Opt.D-PHYTX

Fully-Automated Temperature Chamber testing

- Supports HS tests only
- Setup
 - 4x P75xx probes
 - High Temp Tips (020-2958-xx - Kit of 10)
 - Socket Cable XL (020-2960-xx)



Opt.D-PHYTX Release2

Error Handling

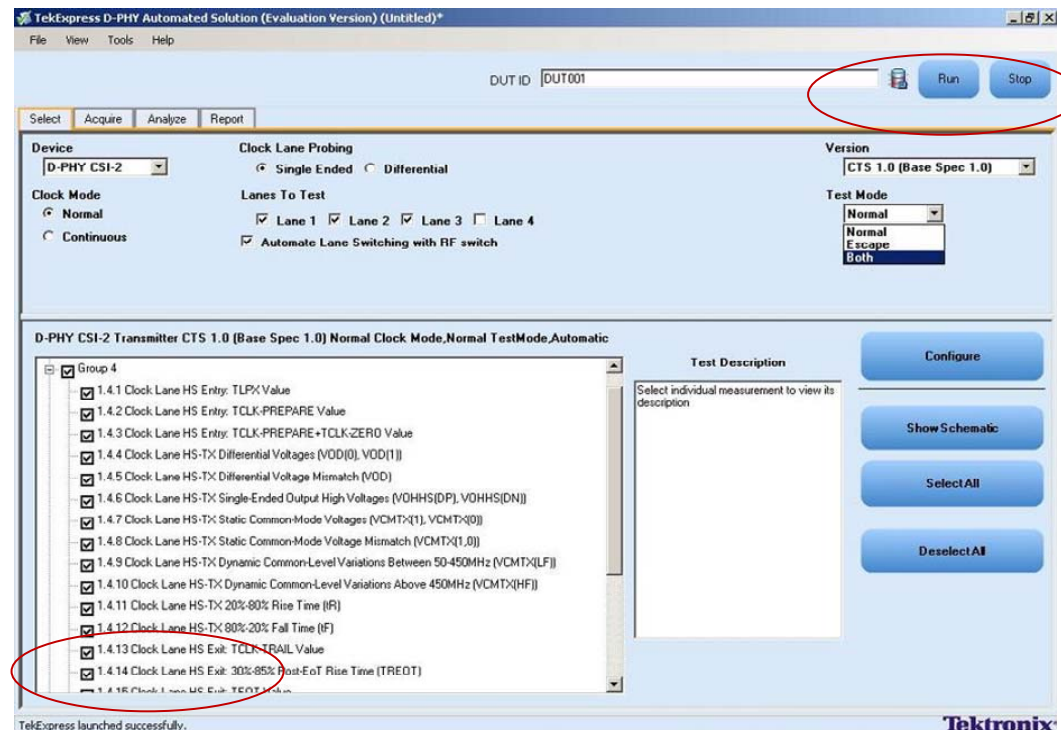
- Test reports with Errors/ Exceptions information help identify Setup/ Acquisition issues quickly

Error code	Error Description
50111	Waveform file not found
50001	Could not find HS region
50002	Could not find LP region
50003	HS UI could not be computed
50004	Pattern 011111/100000 not found
50006	Pattern 111000 not found
50007	Pattern 000111 not found
50008	Possible improper Clock
50009	Could not find HS Trail
50010	Could not find TREOT

Opt.D-PHYTX Release3

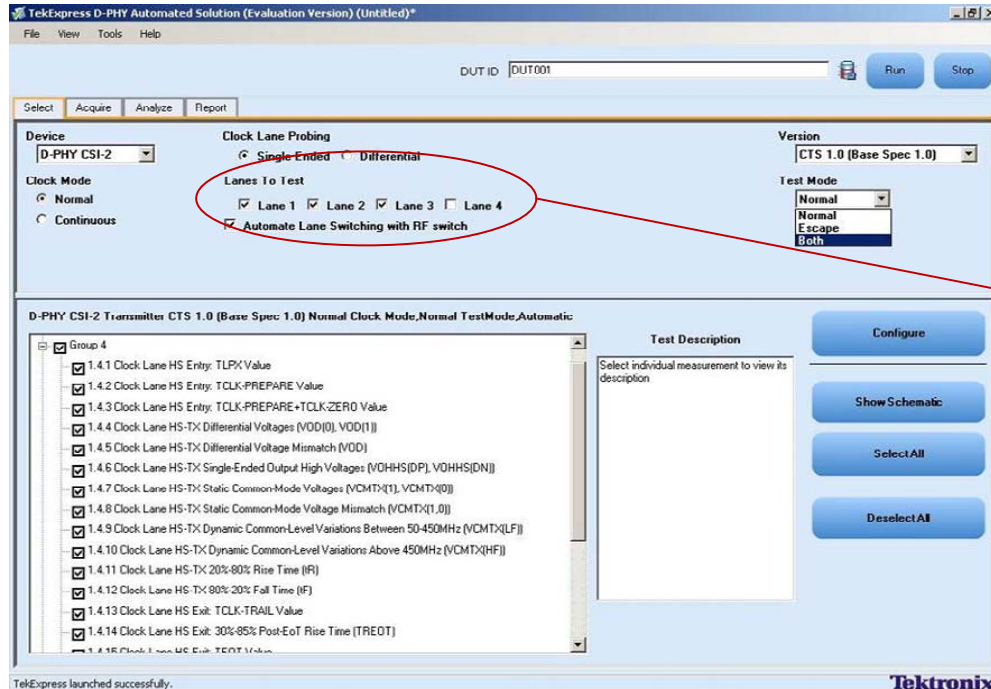
Updated Features & Benefits 1

- **100%** Tests coverage
 - 9 new measurements added (Test IDs: 1.1.5, 1.1.6, 1.1.7, 1.2.5, 1.3.15, 1.3.16, 1.4.15, 1.4.16, 1.5.4)
 - Only automated SW that supports all 49 Tx CTS tests.
- Latest Specifications (v1.0) support
 - Only SW that supports both Base Spec v1.0 and CTS v1.0

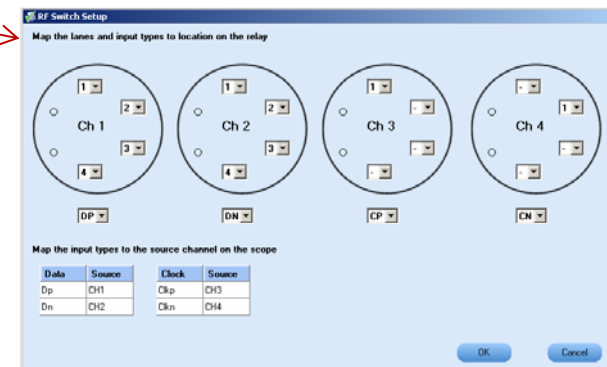


Opt.D-PHYTX Release3 Updated Features & Benefits 2

- Multi-lane Full-Automation using external RF Switch
 - Only solution that supports automation for multilane DUTs.
 - Enables Single-button execution for “multi-lane” DUTs.
 - Provide single-printable report for all lanes together.
 - The results in the report are tabulated lane-by-lane.
 - [Switch: www.keithley.com/products/switch/rfmicrowave/?mn=S46](http://www.keithley.com/products/switch/rfmicrowave/?mn=S46)



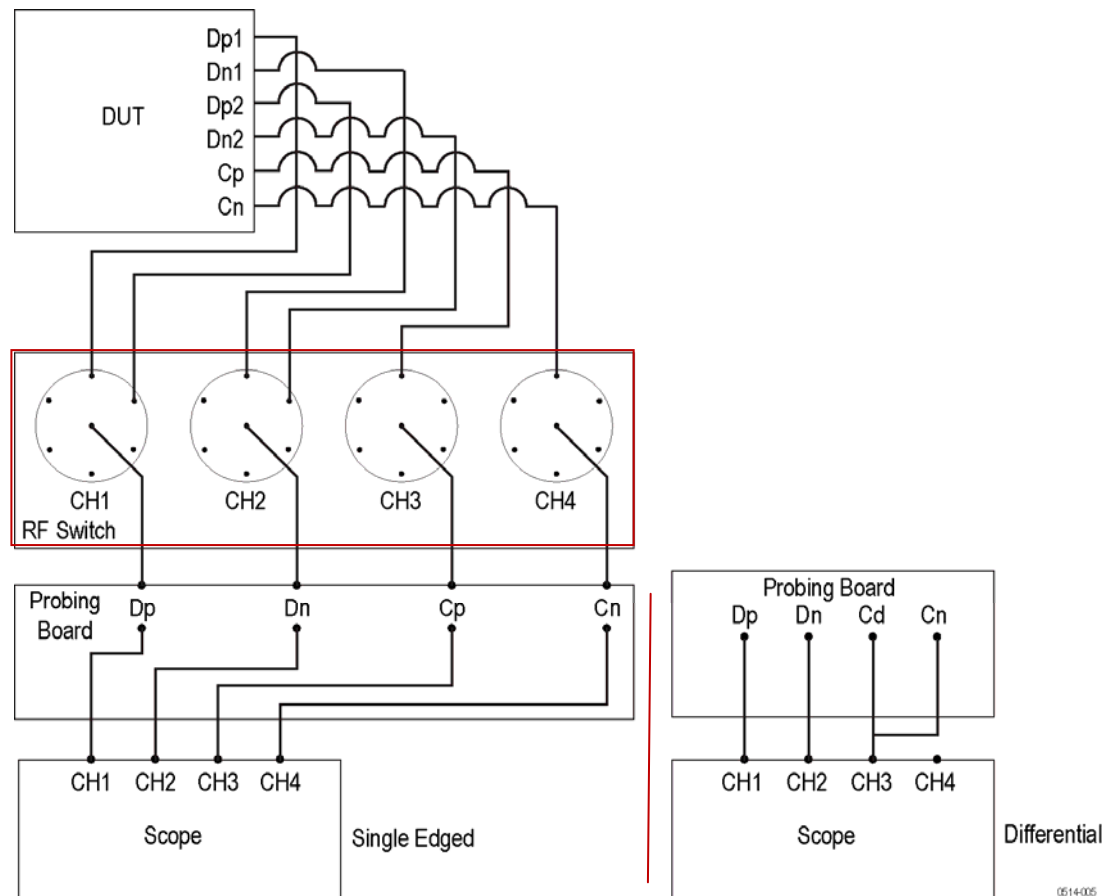
KEITHLEY
Keithley S46 Microwave Switch System



Opt.D-PHYTX Release3

Updated Features & Benefits 2

- Multi-lane Full-Automation Setup Details:
 - Use external RF Switch: www.keithley.com/products/switch/rfmicrowave/?mn=S46
 - Probe using 4x Single-Ended or 3x Differential supported probes



0514-005

Opt.D-PHYTX Release3

Updated Features & Benefits 3

- Improved reports with “Zoom-In” screenshots of the cursors placement for each test.

TekExpress Automation Framework
D-PHY Transmitter Signal Characteristics Test Report

DUT ID : DUT001
 Date/Time : 2/14/2011 16:34
 Device Type : D-PHY
 Execution Time : 7 Min.
 CTS Version : CTS
 Overall Compliance : Pass
 Overall Test Result : Pass

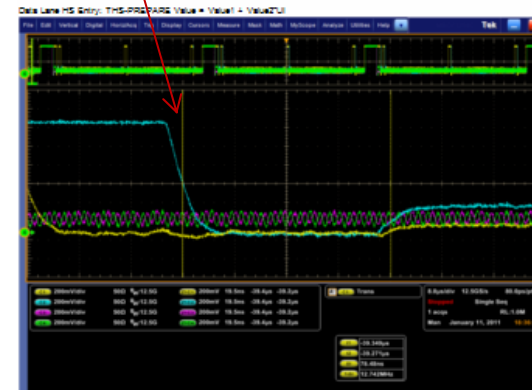
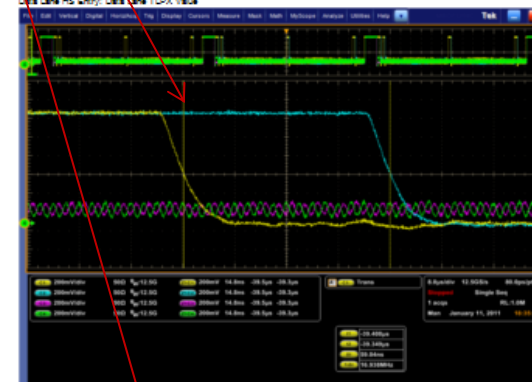
Scope Model : MS070004 Scope Serial Number : Q200002 Scope FW Version : 6.1.1 DEVBUILD 34 SPC_FactoryCalibration : Pass
 OHI Probe Model : 1X OHI Probe Serial Number : N/A TekExpress Version (DUT): 3.0.0.21, Framework: 1.4.6.170
 OHI Probe Model : 1X OHI Probe Serial Number : N/A
 OHI Probe Model : P23135MA OHI Probe Serial Number : SPOOF_1
 OHI Probe Model : N/A OHI Probe Serial Number : N/A

Lane	Test 1	Test 2	Test 3	Test 4	Clock Lane
Status	Pass	Pass	Pass	Pass	N.A.

Computed UWS: 1.951961266

Test Name	Measurement Details	Low Limit	Measured value	High Limit	Margin	Units	Test Result	Compliance Mode	Analysis Time	Mi	Ma
Lane1											
1.5.1 HS Entry TCLK PREValue	HS_Entry_TCLK_PRE Value = Value1 UI	> 14.815514152	102.4800000000	-	87.6645	nS	Pass	Yes	7 Sec	Mi	Ma
Lane2											
1.5.1 HS Entry TCLK PREValue	HS_Entry_TCLK_PRE Value = Value1 UI	> 14.815587968	102.4800000000	-	87.6644	nS	Pass	Yes	6 Sec	Mi	Ma
Lane3											
1.5.1 HS Entry TCLK PREValue	HS_Entry_TCLK_PRE Value = Value1 UI	> 14.815567952	102.5333333333	-	87.7178	nS	Pass	Yes	7 Sec	Mi	Ma

Test Name	Measurement Details	Low Limit	Measured value	High Limit	Margin	Units	Test Result	Compliance Mode	Analysis Time	Mi	Ma
1.3.4 Data Lane HS-TX Differential Voltages (VDDQ1, VDDQ11)											
	Lane2						Pass	Yes			
							Fail	No			
1.3.5 Data Lane HS-TX Differential Voltage											
	Lane1						Pass	Yes			
							Fail	No			
1.3.6 Data Lane HS-TX Differential Voltage											
	Lane2						Pass	Yes			
							Fail	No			



D-PHY Tx Testing Solution – Continued

■ Fixtures

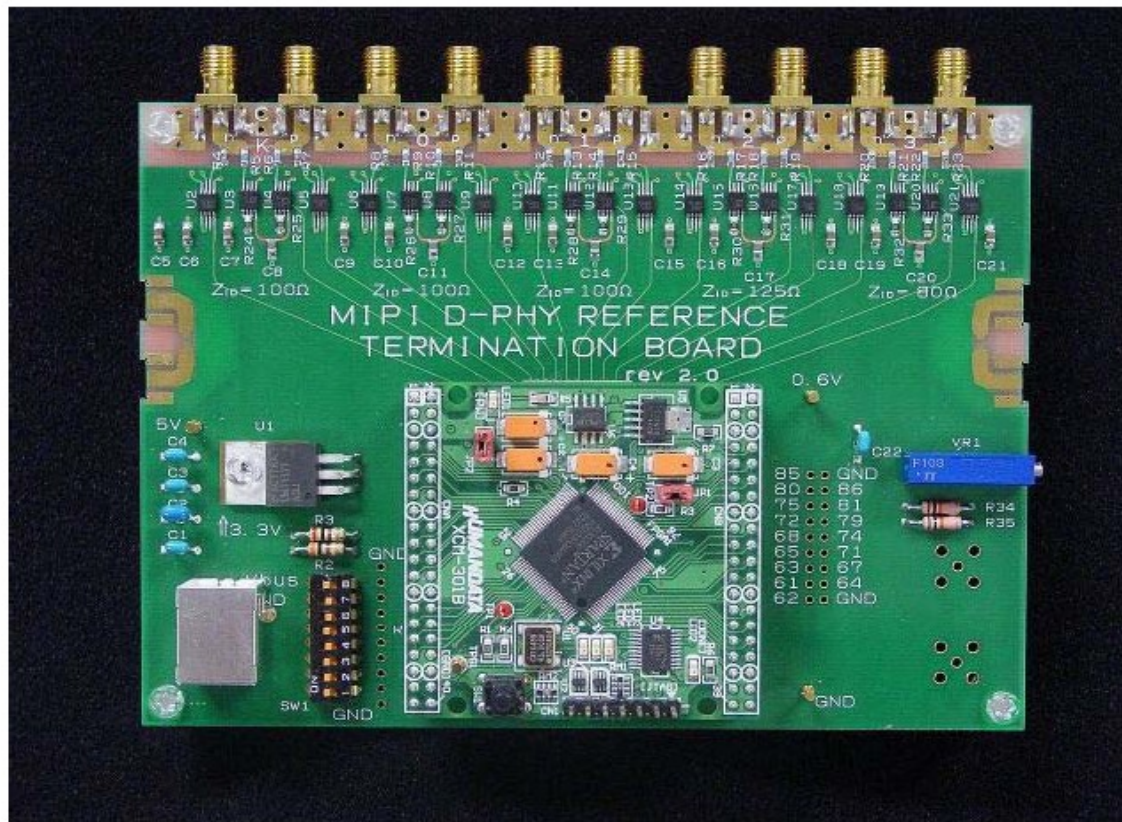
- Issue with HS vs. LP termination, Z id load variation, C load
- Ideally, fixture would provide active reference termination
- Solder-in high impedance SE probes or DIFF probes connected for SE are best for in-situ test
- **No standard fixture defined by MIPI**
- **Tektronix Recommendation:**
 - **Follow guidance and purchase as necessary from UNH-IOL**
 - MIPI D-PHY Reference Termination Board \$2,395.00
 - MIPI TLIS Board \$795.00
 - MIPI D-PHY Probing Board \$450.00
 - SMA Alignment Fixture \$95.00
 - SMA Couplers \$9.00
 - http://www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc

■ Test Data Generation

- Vendor specific
- **No standard test pattern generation defined**

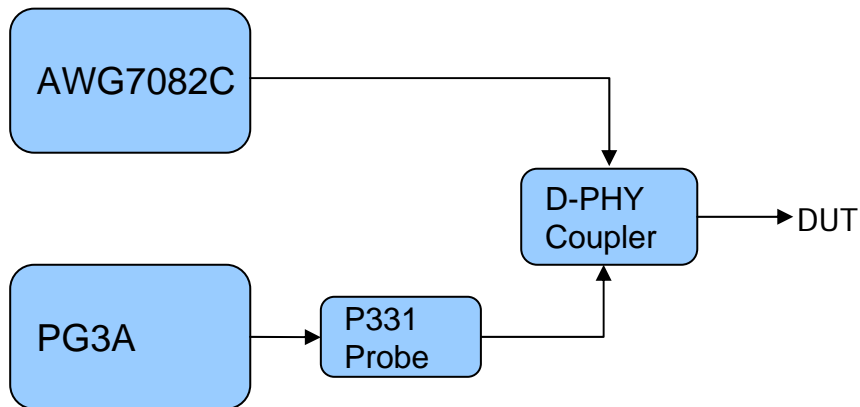
D-PHY Tx Testing Solution – Continued

MIPI D-PHY REFERENCE TERMINATION BOARD (RTB) OVERVIEW AND DATASHEET



D-PHY Rx Testing Solution

- Require generation of SE signals
- Recommend: PG3A Pattern Generator from Moving Pixel
 - PG3ACAB (External module), Or, PG3AMOD (Plug-in for TLA)
 - DPhy-P6980
 - P331 or P375
- Alternatives:
 - DTG5078 with Pattern Gen files
 - AWG7052 or AWG7102 for D-PHY &M-PHY



PHY Specification History

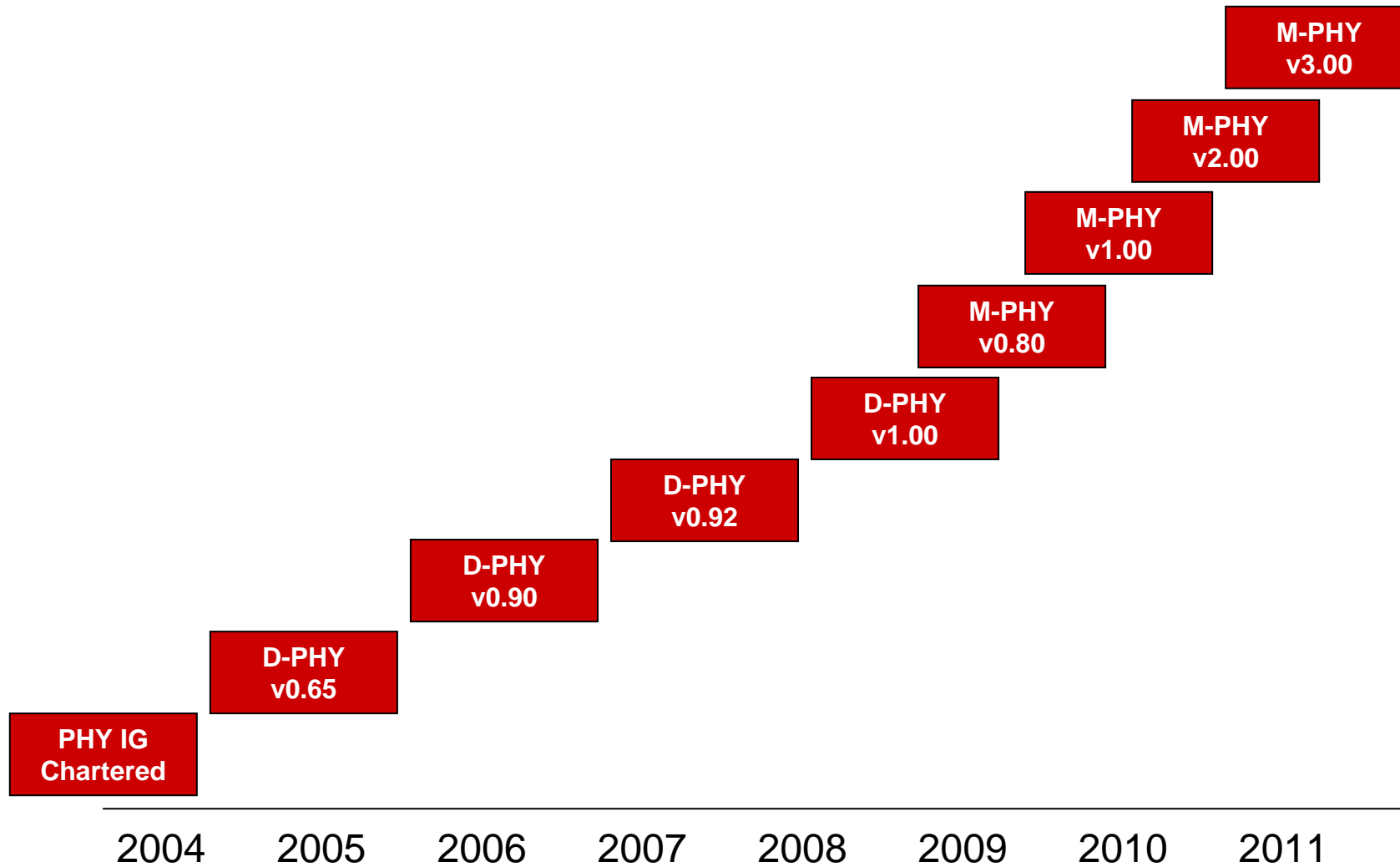


Chart courtesy of MIPI Alliance

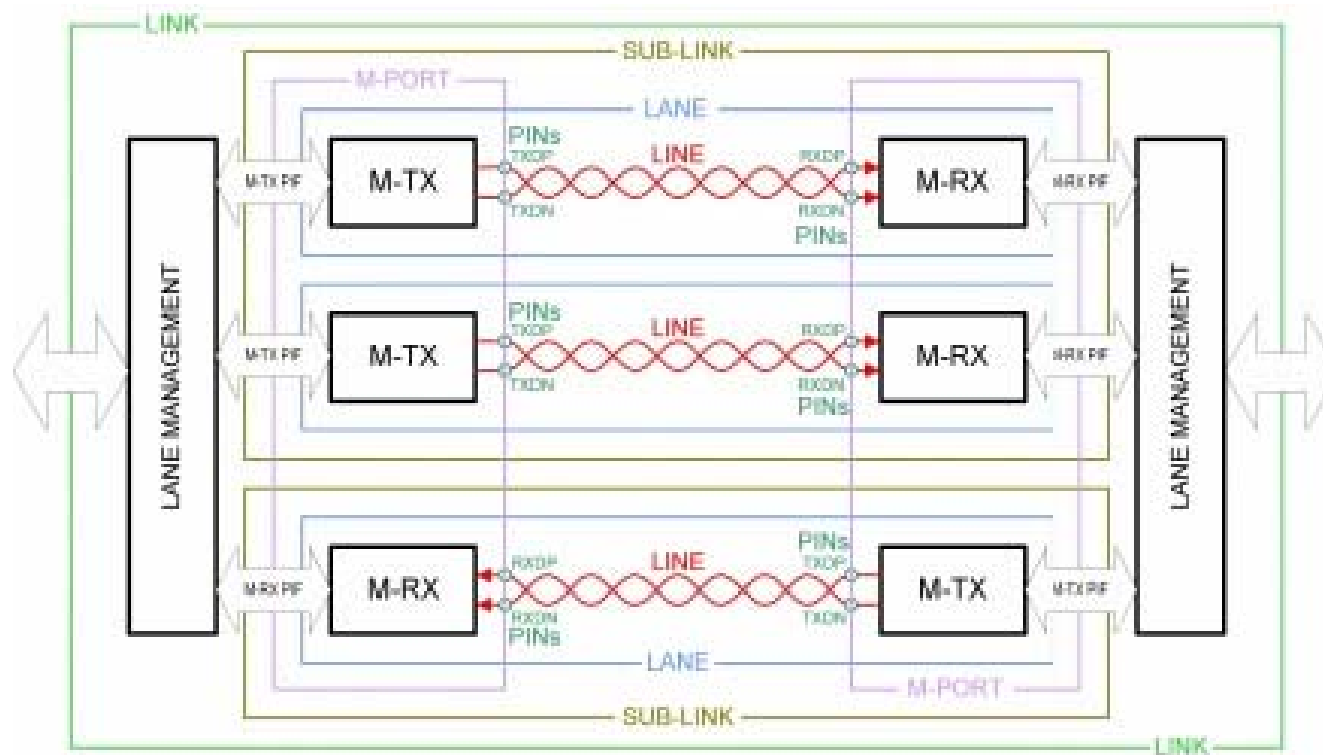
What is M-PHY ?

- M-PHY is a flexible architecture that allows the implementer to support high data rates at minimal power, cost & I/O redesign
- Brings to the mobile device industry an optimized chip-to-chip spec for High Definition Video, large Internet data traffic loads

		D-PHY	M-PHY
Min. # of pins per direction		4	2
Min. # of pins for Min. configuration		4	4
		only unidir or half-duplex	dual-simplex
Data rate per lane	HS	>80 Mb/s (Practical limit 1Gb/s)	~ 1¼ , 2½ , 5 Gb/s ~ 1½ , 3 , 6 Gb/s
	LS	< 10 Mb/s	10k-600Mb/s
Electrical signaling	HS	Diff (200mVpk)	Diff (200/120mVpk)
	LS	LVC MOS1.2V	Diff (400/240mVpk)
HS Clocking method		DDR Source-Sync Clk	Custom Clk
Line coding		None or 8b9b	8b10b
Power – Energy/bit		Low	Lower

M-PHY Architecture

- A Fast, Scalable, Serial Communications Architecture
 - Link – Connects M-PHY Transmitter to an M-PHY Receiver
 - Sub-link – Manage one or more lanes
 - Lane – Operation defined in the protocol (DSI, CSI, UniPro, DigRF)



M-PHY Testing Challenges

Signaling Mode	Speed	Level (V)	Impedance
M-PHY-PWM	576Mbps	500e-3/250e-3 260e-3/130e-3	10k/50 ohms
M-PHY-SYS	576Mbps	500e-3/250e-3 260e-3/130e-3	10k/50 ohms
M-PHY-HS	5.83Gbps	250e-3/130e-3	50 ohms

- Higher data rate will increase importance of Signal Integrity of links
 - Acquisition capability of oscilloscope will need to increase
 - More emphasis on timing/jitter and noise (signal integrity)
 - Receiver testing will be needed to stress-test resulting BER

M-PHY signaling scheme

- Non-Return-to-Zero (NRZ)
- Pulse Width Modulation

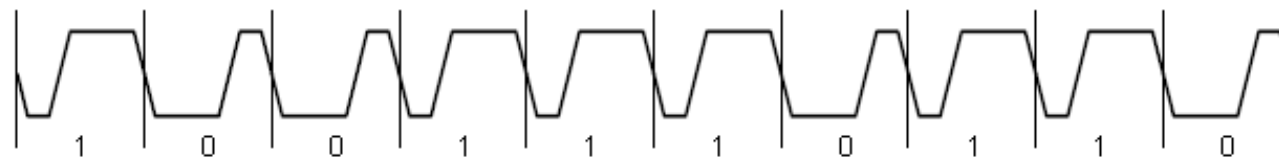
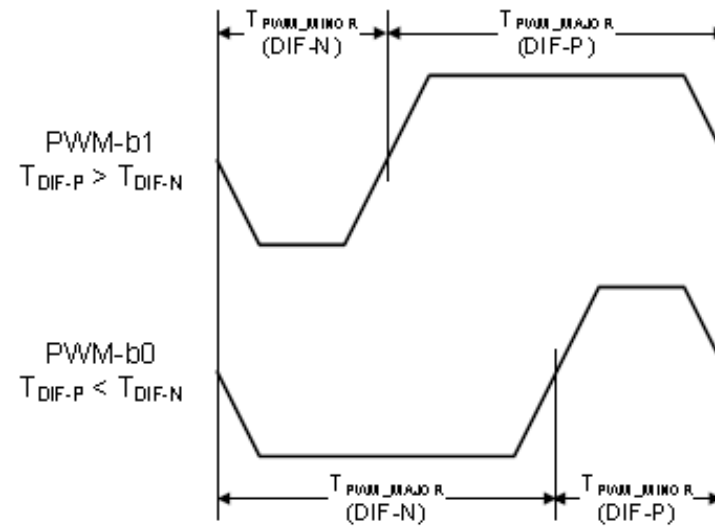


Figure 4 PWM Bit Waveforms and Bit Stream Example



M-PHY Physical Layer Testing Solution

- Oscilloscopes
 - DPO70604B for HS-GEAR1
 - DPO/DSA/MSO70804 for other HS-GEARs
 - For risetime (70ps) measurements within +/-5% of spec
- Probes
 - Recommend:
 - **2x P73xxSMA or P73xx or P75xx per each Lane**
 - TDPxx can support limited HS Gears
 - Probing Considerations
 - Two types of terminations - Restive terminated, and not Terminated.
 - LS mode can operate either terminated or not terminated
 - HS mode it is always terminated, so the swing are halved.
- Signal Generators
 - AWG7112B
- Software
 - DPOJET Timing and Analysis with M-PHY setup files and MOIs*
 - ERRDT Scope Error Detector
 - SerialXpress Software for AWG.
 - DigRFv4 Decode Software from Moving Pixel



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Tektronix Supported by UNH-IOL For D-PHY & M-PHY Conformance Testing

The screenshot displays a Windows desktop environment. On the left, an Internet Explorer browser window titled "MIPI Alliance - Workspace" is open to the URL <https://members.mipi.org/mipi-testing/workspace/StartPage>. The page content includes "D-PHY Testing Resources:" with sections for "Test Suite Documents:" (listing "D-PHY Physical Layer Conformance Test Suite (v0.08)") and "Test Tools:" (listing "DPHYGUI: Waveform Conformance & Analysis Software (v20090507)"). A red diagonal watermark reads "MIPI Alliance Member Confidential Web Page".

In the center-right, a window titled "DPHYGUI: D-PHY TX Test Tool (v20090507)" is open. The main title is "MIPI D-PHY TX Signal Analysis And Conformance Tool". It features a sidebar with buttons for "CSI/DSI Decoder", "HS Burst Tests", "HS Clock Tests", "LP Tests", "Plot PSD", "Plot TDR RLoss", "Plot TLIS IL/RL", "Plot TLIS NEXT", and "TX Signal Sim". The main area contains configuration options: "Decoder Mode" (radio buttons for CSI and DSI), "Reference Clock Format" (radio buttons for Single Differential Waveform, Two Single-Ended Waveforms, and None), "Software CDR Type" (radio buttons for Linefit and Edge2Edge), and "Misc Debugging Options" (checkboxes for Truncate imported data, Enable LPF test filter, Plot imported data, then abort, and Enable burst timing debug plot).

In the foreground, a Notepad window titled "README and Rev Log - Notepad" is open, displaying the following text:

```
File Edit Format View Help

core measurement algorithms described in the test suite. It performs
measurements on arrays of sampled waveform data, and currently supports
Agilent (.bin), Tektronix (.wfm) Lecroy (.trc), and MATLAB (.mat) formats.
This code does not include capability for acquiring/downloading data directly
from a scope (e.g., via GPIB/LAN, etc). The code may be modified to support
additional data file types in future revisions.
```

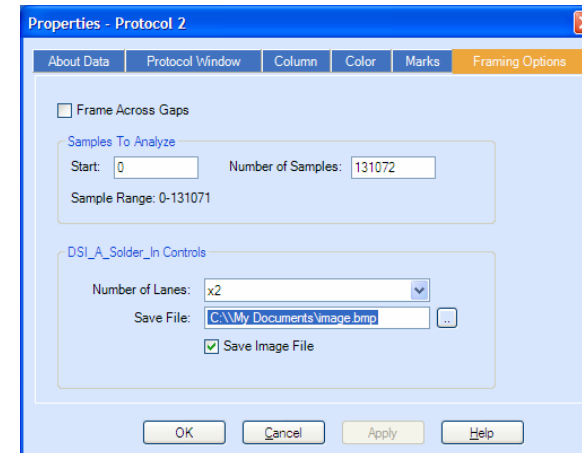
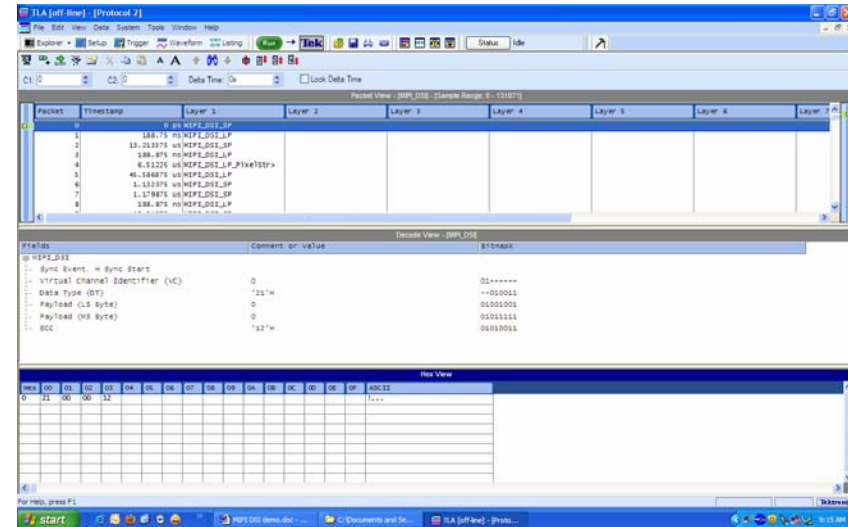
CSI/DSI HS Data Listing for Logic Analyzer

- Low Level Protocol
 - Disassemble & Display of data (4 lanes) and clock
 - For Link widths of less than 4 user has option to select Lower Link Width
 - Decode & Display LP & HS transition states
 - Display HS Data in Byte Format
 - Suppression of idle cycles for easy analysis

Sample	MIPI_DSI Lane0 State	MIPI_DSI LP_Data	MIPI_DSI LP_Data0	MIPI_DSI LP_Data1	MIPI_DSI LP_Data2
524	HS-Prepare	00000000	00	00	00
525	HS-Prepare	00000000	00	00	00
526	HS-Prepare	00000000	00	00	00
527	HS-Prepare	00000000	00	00	00
528	HS-Prepare	00000000	00	00	00
529	HS-Request	01000000	01	00	00
530	HS-Request	01000000	01	00	00
531	HS-Prepare	00000000	00	00	00
532	HS-Prepare	00000000	00	00	00
533	HS-Prepare	00000000	00	00	00
534	HS-Prepare	00000000	00	00	00
535	HS-Prepare	00000000	00	00	00
536	HS-Prepare	00000000	00	00	00
537	HS-Prepare	00000000	00	00	00
538	HS-Prepare	00000000	00	00	00
539	HS-Prepare	00000000	00	00	00
540	HS-Prepare	00000000	00	00	00
541	HS-Prepare	00000000	00	00	00
542	HS-Prepare	00000000	00	00	00
543	HS-Prepare	00000000	00	00	00
544	HS-Prepare	00000000	00	00	00
545	HS-Prepare	00000000	00	00	00
546	HS-Prepare	00000000	00	00	00
547	HS-Prepare	00000000	00	00	00
548	HS-Prepare	00000000	00	00	00
549	HS-Prepare	00000000	00	00	00
550	HS-Prepare	00000000	00	00	00
551	HS-Prepare	00000000	00	00	00
552	HS-Prepare	00000000	00	00	00
553	HS-Prepare	00000000	00	00	00
554	HS-Prepare	00000000	00	00	00
555	HS-Prepare	00000000	00	00	00
556	HS-Prepare	00000000	00	00	00
557	HS-Prepare	00000000	00	00	00
558	HS-Prepare	00000000	00	00	00
559	HS-Prepare	00000000	00	00	00
560	HS-Prepare	00000000	00	00	00
561	HS-Prepare	00000000	00	00	00
562	HS-Prepare	00000000	00	00	00
563	HS-Prepare	00000000	00	00	00
564	HS-Sync	00000000	00	00	00
565	HS-Sync	00000000	00	00	00
566	HS-Sync	00000000	00	00	00
567	HS-Sync	00000000	00	00	00
568	HS-Sync	00000000	00	00	00
569	HS-Sync	00000000	00	00	00
570	HS-Sync	00000000	00	00	00
571	HS-Sync	00000000	00	00	00
572	Lane0 HS-Data: 0x15	00000000	00	00	00
573	--	00000000	00	00	00

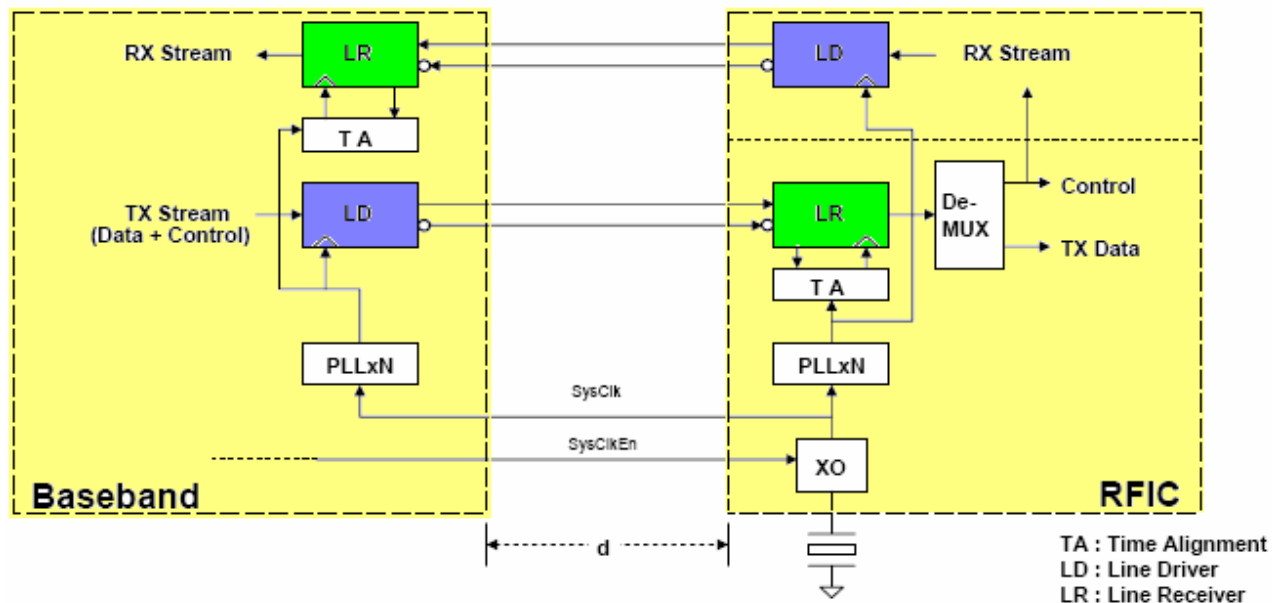
CSI/DSI HS Data Protocol for Logic Analyzer

- Packet by packet view of data
- Decode & Display Long & Short packets
- Payload data decoded
- Payload extracted & stored for further analysis
- Packet data can be exported and saved as Bitmap Image



DigRF – Standard & Testing Support

- Inter-Chip specification for connecting Baseband IC to RF IC
 - Protocol Layer Debug/Validation
 - Physical Layer Debug/Validation
- RF-IC Validation
 - Protocol Layer Validation
 - Physical Layer Validation



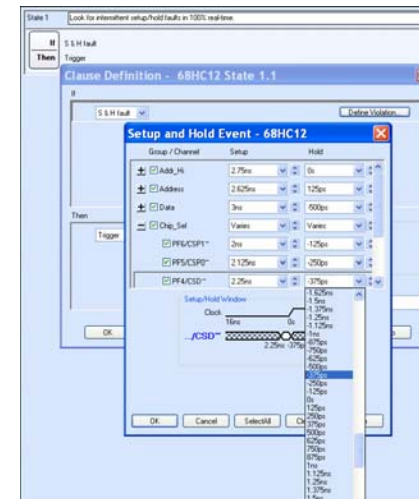
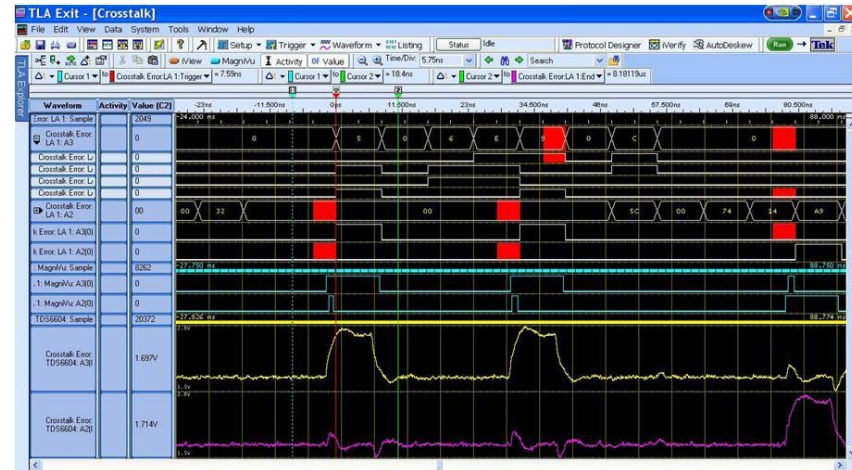
Analysis – Signal Integrity

- DPOJET Jitter and Timing Analysis Software provide the highest accuracy and lowest noise jitter measurements available
- Identifies rare anomalies or glitches in seconds with Real-Time DPO acquisition
- Most complete trigger system in the industry
- User customizable User Interface



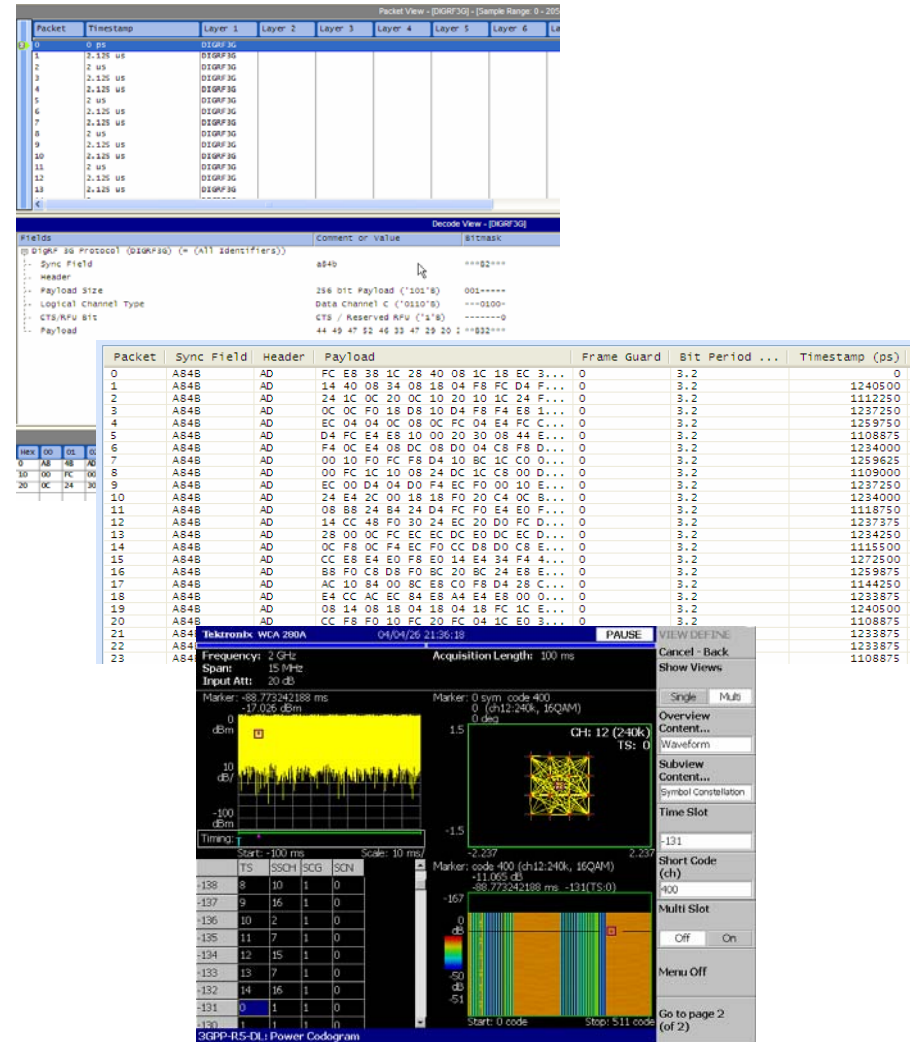
Analysis – Digital Verification & Debug

- Glitch Capture & Display
 - Only LA to trigger on glitches and display their location
- Set Up & Hold Trigger & Display
 - Only LA to trigger on these type of violations and display their location
- 125ps Timestamp resolution
 - Highest resolution LA will find more glitches
- Support packages for uP and Memory devices
 - Complete analysis of the Baseband design



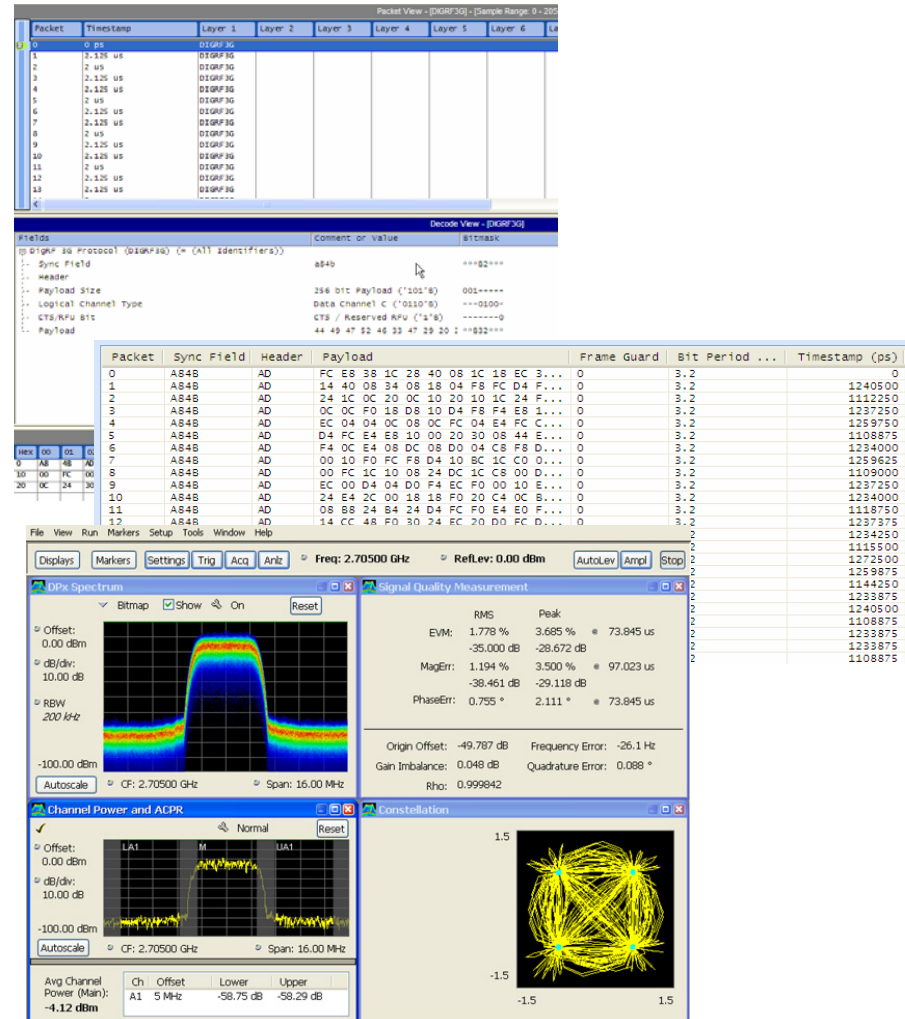
Analysis – DigRF Verification & Debug

- DigRF packets decoded and displayed
- Ability to Search & Filter on fields within DigRF packets
- Flexible data extraction for complete analysis
 - Extract IQ data for Modulation Analysis
 - Extract sync, header & payload data
- Transitional mode acquisition



Analysis – DigRF Verification & Debug

- Seamless integration between Digital and Modulation Domains
 - IQ is automatically extracted and loaded into RSAVu
- No specialized hardware or probing is required
- Customizable, allowing propriety and non compliant DigRF signals to acquired and analyzed
- DigRF solution is available free of charge

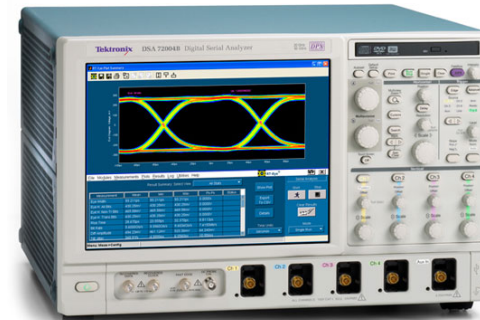


Summary - Tektronix MIPI Testing Support

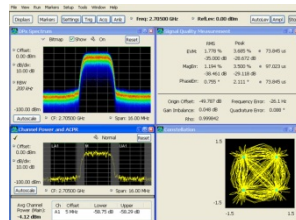
CSI/DSI Protocol & Logic Analysis



D-PHY & M-PHY/ Physical Layer Analysis



DigRF Verification & Debug



CSI/DSI Pattern Generation



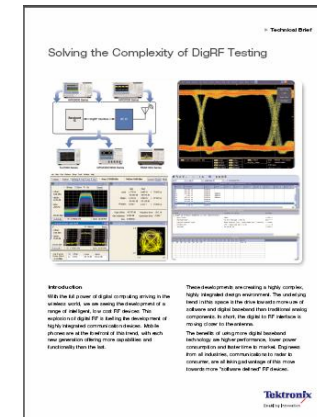
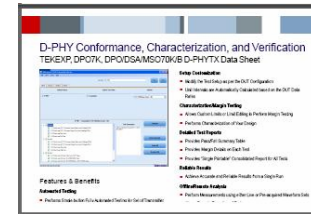
Additional References

www.Tek.com/MIPI:

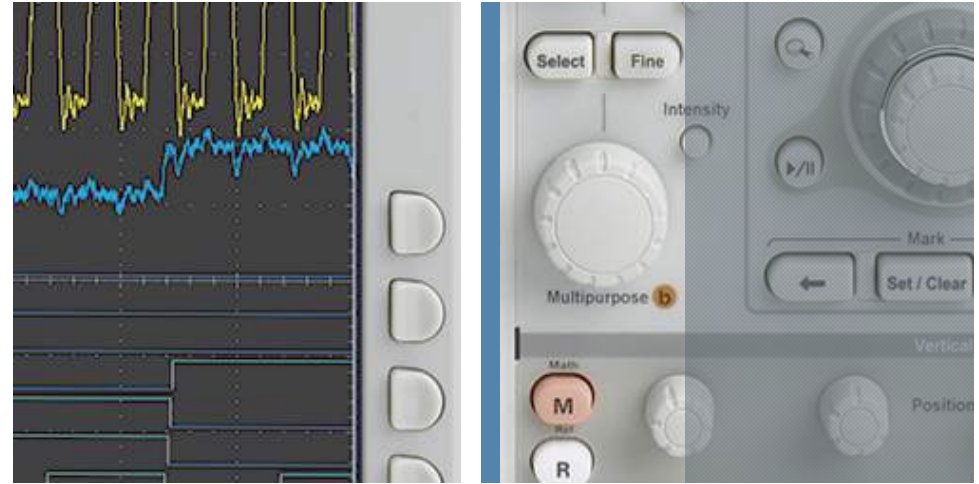
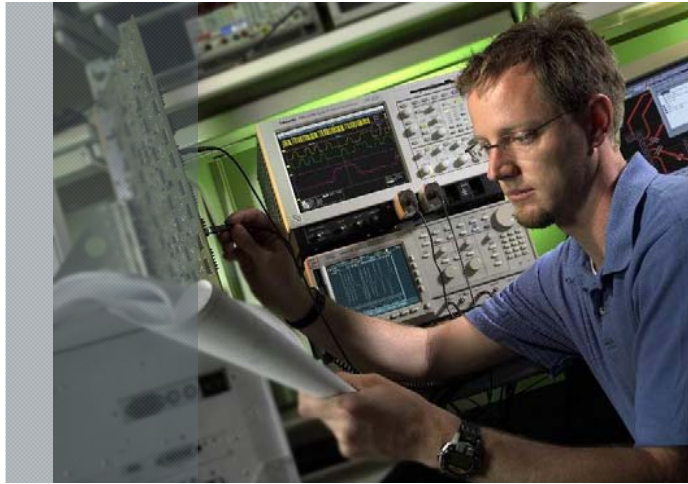
- D-PHY Datasheet
- D-PHY/ CSI/ DSI Application Note
- DigRF Application Note
 - <http://www2.tek.com/cmswpt/tidetails.lotr?ct=TI&cs=tbr&ci=11854&lc=EN>
- Fact Sheet:
 - <http://www2.tek.com/cmswpt/pidetails.lotr?ct=PI&cs=psa&ci=15031&lc=EN>
- Opt. D-PHY MOI
 - http://www.tek.com/applications/computing/serial/recommended_equipment.html#mipi
- DPOJET Analysis Tool
 - http://www2.tek.com/cmsreplive/psrep/13555/61W_21170_3_2010.04.16.08.11.57_13555_EN.pdf

Other:

- D-PHY Conformance Test Spec (CTS):
 - Rev 0.98: [https://members.mipi.org/mipi-testing/file/UNH-IOL/UNH-IOL%20Test%20Suite%20Documents/DPHY/MIPI_D-PHY_Conformance_Test_Suite_\(v0.98\).pdf](https://members.mipi.org/mipi-testing/file/UNH-IOL/UNH-IOL%20Test%20Suite%20Documents/DPHY/MIPI_D-PHY_Conformance_Test_Suite_(v0.98).pdf)
 - Rev 0.08: [https://members.mipi.org/mipi-testing/file/UNH-IOL/UNH-IOL%20Test%20Suite%20Documents/DPHY/MIPI%20D-PHY%20Conformance%20Test%20Suite%20\(v0.08\).doc](https://members.mipi.org/mipi-testing/file/UNH-IOL/UNH-IOL%20Test%20Suite%20Documents/DPHY/MIPI%20D-PHY%20Conformance%20Test%20Suite%20(v0.08).doc)
- MIPI Alliance Video on Tek Solutions
 - <http://www.youtube.com/watch?v=Mf9rv-X2YG4&feature=channel>



Thank You



Tektronix[®]