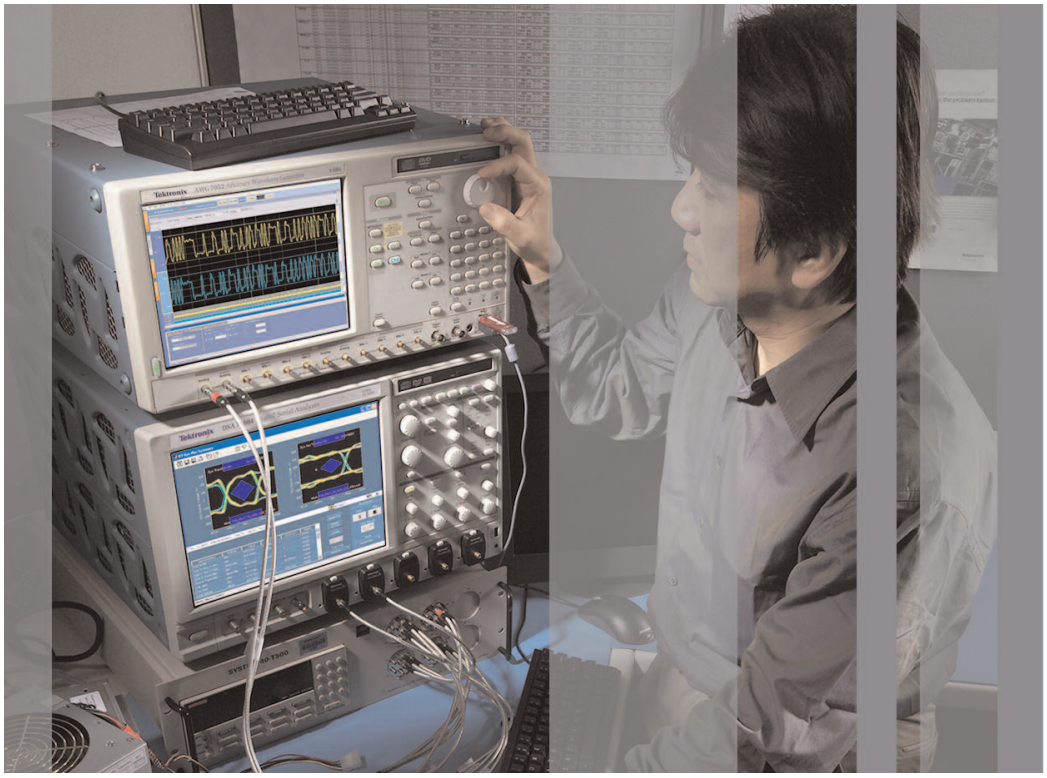
Application Note



Overcoming High Speed Serial Data RX Testing Challenges Using an AWG and Direct Synthesis

Tektronix®

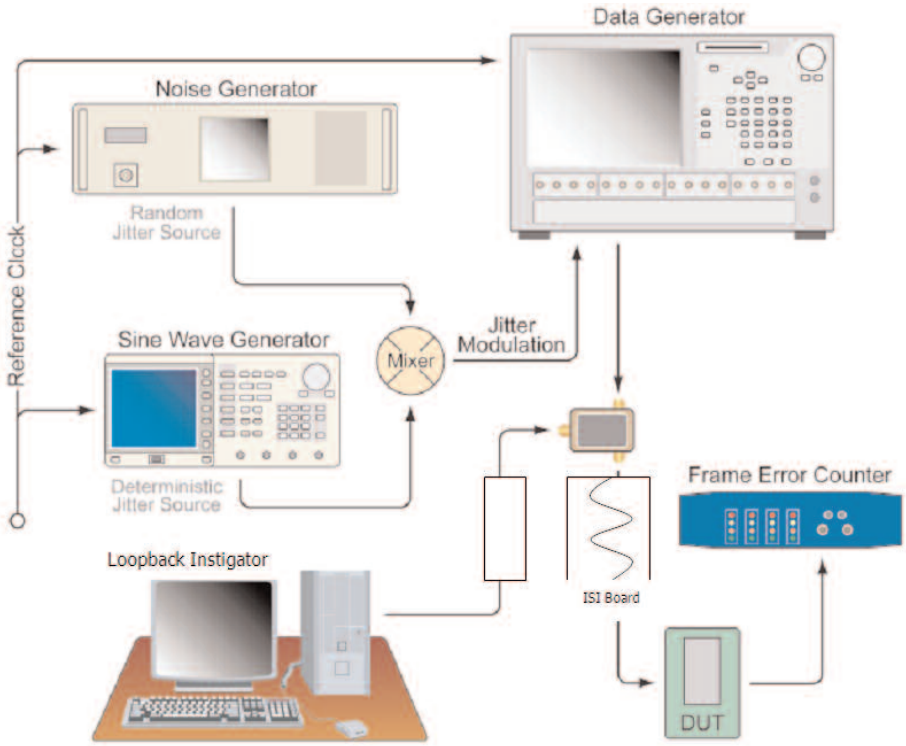


Figure 1. Old RX testing configuration.

Serial Data is the Heartbeat of Digital Data Applications

With digital data becoming prevalent in all forms of consumer products today. High Speed Serial Data testing is one of the biggest challenges for the design and test of these popular devices. From products that range from video games to high end PCs, Serial Data is the heartbeat of this digital data revolution. In order for consumers to be guaranteed that their new flat panel screen will work with their new High Definition enabled PC, manufactures must test this “heartbeat” of the digital data components. Just as we test our heartbeat under stress to verify a healthy body, digital designers must also stress serial data designs to verify they can handle real world conditions that will be encountered.

For this application note we will focus on DisplayPort as the digital data application, but the techniques described here can also be used in other applications such as PCI Express, SATA, HDMI and many more.

DisplayPort application Example

DisplayPort is a new digital interface proposed to deliver digital display content to PC displays, monitors and future Consumer Electronic devices. DisplayPort is destined to replace analog forms of display technologies such as VGA that is used in most PCs today. It will also replace the digital interface DVI since DVI does not support audio. This new architecture will enable display system manufacturers the ability to provide true digital display capability without requiring Analog to Digital or Digital to Analog conversions. It will also provide chip to chip data flow for mobile/lap top configurations or box to box capability using a single interface. DisplayPort enables both video and audio content to be delivered through this 8b10b high speed serial data stream. See Figure 1.

Receiver Testing Requirements

Along with most serial data applications DisplayPort requires elaborate receiver stress testing. In order to guarantee that these high data rate signals can be correctly recovered through cables, connectors and FR4 board traces, receiver PLL and clock recovery circuits need to be able to handle noisy or stressed signals. The specific requirements are defined in the DisplayPort Compliance Test Specification (CTS), but this specified stressed signal is comprised of periodic jitter, random jitter and ISI components added to the serial data test pattern being transmitted. The output data is then verified to see if any errors occur during the transmission of this stressed signal.

Receiver Testing Equipment Challenges

In order to generate these specified stressed test patterns complex test and measurement configurations have been used. These configurations usually are comprised of pattern generators in conjunction with sinewave generators, noise generators and external cable emulators or FR4 board traces. All of these sources are combined in order to provide the final stressed signal.

These test configurations are expensive, require complex calibration routines and are very difficult to duplicate. With this configuration the ISI content has to added using an external cable emulator or an external FR4 board, each generator has to be calibrated for its specific content allowing for losses associated with the RF splitter used to combine all these signals and in some cases a PC used to put the device into a test or loopback mode. As you can imagine even with these complex configuration some tests can not be completed because of generator specification limits or configuration issues. For instance lets look at the DisplayPort CTS. At the time of this writing the required stressed receiver test comprised of the following methodology.

1. Send a Frequency Lock D10.2 pattern
2. Send a Symbol Lock (K28.5, D11.6, D10.2) pattern
3. Send a clean PRBS7 pattern
4. Clear the error counter using the Aux channel
5. Send a Single bit error applied to the PRBS pattern to verify error counter operation
6. Clear the error counter again
7. Send a PRBS7 output with specified Rj, Sj, and ISI content
8. Run for prescribed time and verify number of bit errors through the Aux channel

DisplayPort supports two data rates. The slower or Reduced Bit Rates (RBR) (see Table 1) operates at 1.62Gb/s and High Bit Rate (HBR) (see Table 2) mode runs at 2.7Gb/s. It also supports up to 4 lanes of traffic.

f(sj)	Tj(JTRBRrx)-10%	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1648	570	7.9	981
10	778	570	7.9	111
20	747	570	7.9	80

Table 1. Jitter Component Settings for Reduced Rate.

f(sj)	Tj(JTHBRrx)-10%	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1079	161	13.2	756
10	509	161	13.2	186
20	489	161	13.2	166
100	484	161	13.2	161

Table 2. Jitter Component Settings for High Rate.

Each lane that is available will be tested using each of these Sinusoidal jittered frequency components along with the specified Random Jitter and ISI. Notice the high jitter amplitude of 953 mUI required for the 2 MHz SJ component. Also notice the high ISI content required for all of the RBR and HBR tests. These specific requirements enable the DisplayPort standard to guarantee as part of the “LOGO Test” requirements that if a vender displays the DisplayPort logo, the product has passed this test and has verified it will even work with lossy cables or connectors. The reduced bit rate jitter tolerance test includes the most difficult requirements for the receiver test generation techniques described above. Also verification and calibration of the equipment becomes challenging because the total jitter content is greater than one Unit Interval (UI). This poses a challenge for most jitter measurement equipment. In order to guarantee the correct amount of jitter is being generated the jitter should first be calibrated.

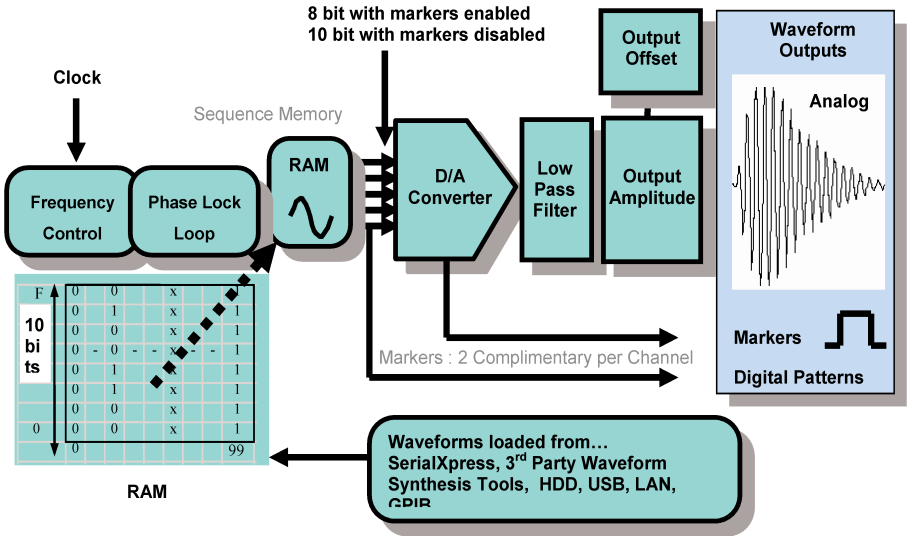


Figure 2. Simplified diagram of AWG.

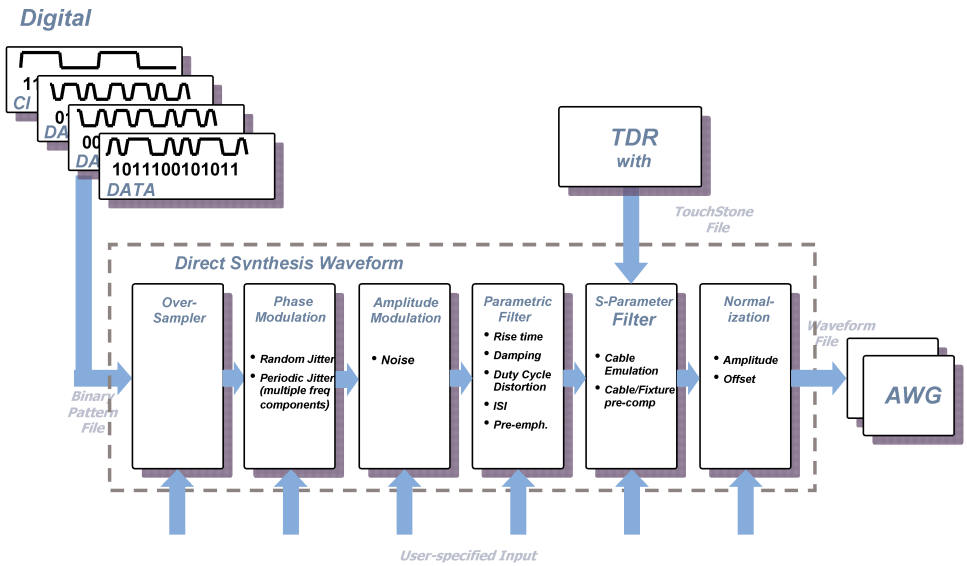


Figure 3. Tektronix Direct Synthesis components.

AWG Simplified Method for RX Testing

The introduction of Arbitrary Waveform Generators (AWGs) with a sample rate up to 20GS/s (see Figure 2) has enabled a change in the test equipment configurations for these receiver tests. Using the Direct Synthesis technique the AWG becomes the perfect tool for complex jitter stress test challenges.

Since the AWG generates analog signals, it is the perfect tool to generate High Speed Serial Data stressed signals without the configuration nightmares of the multiple generator setups and external cable emulators and time transition converters. Because of the 20GS/s capability, the max 2.7Gb/s data rate of DisplayPort can be oversampled thus enabling jitter and transmission channel effects such as ISI to be synthesized directly into the data that is generated through the Digital to Analog Converter (DAC). This is the basic definition of Direct Synthesis methodology. (see Figure 3)

To have the AWG's hardware capability is important, but not the only piece of the Direct Synthesis solution. Software to create the waveforms is a critical part of the equation.

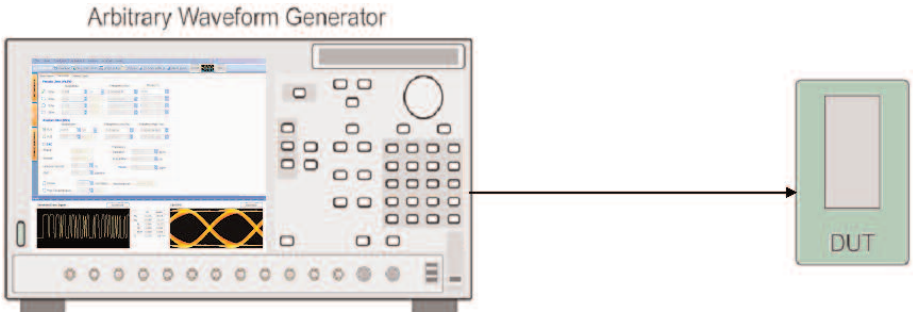


Figure 4. New RX testing solution.

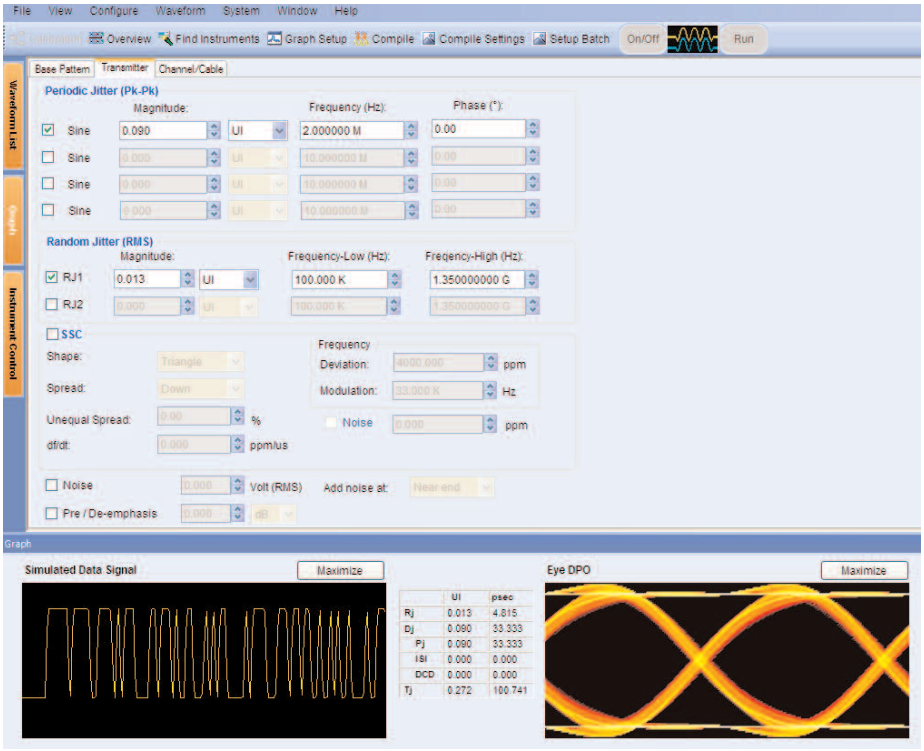


Figure 5. SerialXpress® user menu.

SerialXpress® Enables the Complete Solution

Building these stressed signals is not a trivial matter and understanding the AWG s architecture is required in order guarantee the generated signals are correct. SerialXpress® makes creation of these signals a simple process and enables the full RX testing solution all from one instrument. See Figure 4.

SerialXpress® allows the user to choose a base pattern from many of the serial data standards such as DisplayPort, PCIe, SATA, HDMI Fiber Channel etc. and then specify the specific amounts of SJ, RJ, Noise or Pre-emphasis. SerialXpress® also allows emulation of any kind of channel/cable effects and synthesize these effects together with the test signal. See Figure 5. Using specific ISI values or use S-Parameters from a TouchStone file that was acquired from a known transmission channel these effects can be easily included.

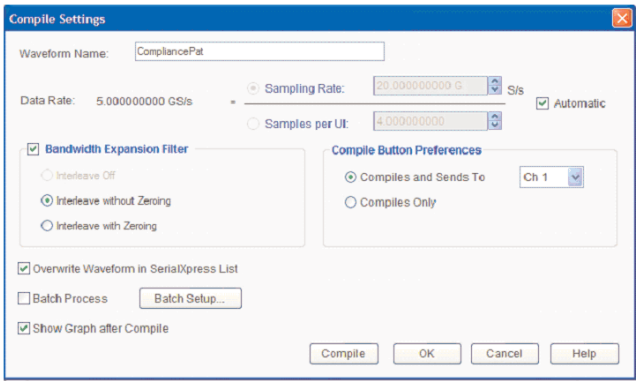


Figure 6. Channel/Cable settings menu.

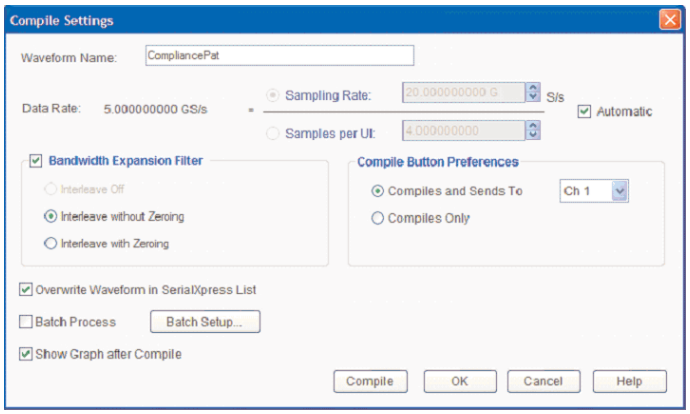


Figure 7. Compile settings and Bandwidth Expansion filter menu.

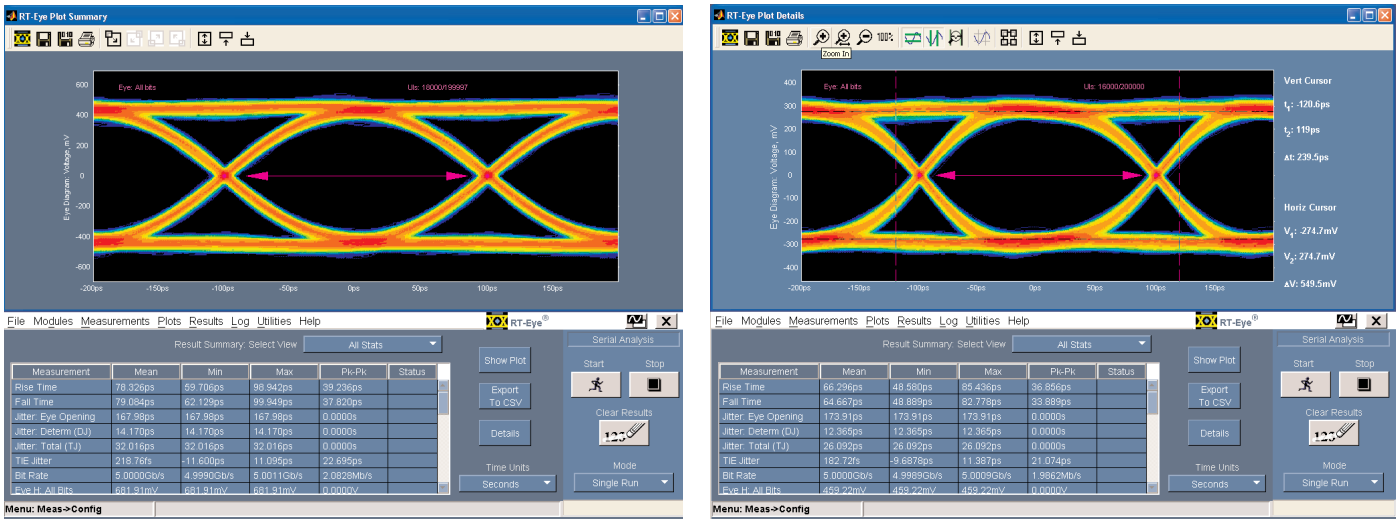


Figure 8. PRBS7 signal before and after Bandwidth Expansion filter feature applied.

SerialXpress® also has a patented ISI Scaling feature that allows for a virtual cable length adjustment of the captured S-Parameters. See Figure 6. Spread Spectrum Clocking insertion enables SerialXpress® to be a full featured Direct Synthesis generation tool that fulfills all the requirements for Serial Data testing.

For standards that require faster rise times such as SATA Gen III at 6Gb/s, SerialXpress® incorporates a patented digital filter that improves the synthesized waveform s rise time and bandwidth. See Figures 7 and 8.

Automated Calibration

SerialXpress® incorporates an automated calibration procedure that uses a connected Tektronix oscilloscope to verify that the AWG generated output of the Direct Synthesized content is what the user expected.

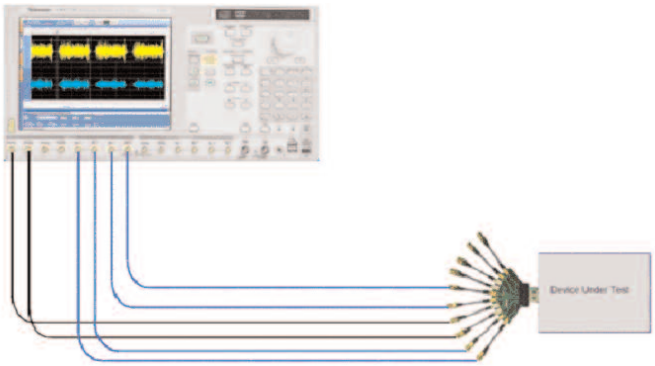


Figure 9. AWG Marker configuration for adjacent lane aggressor testing.

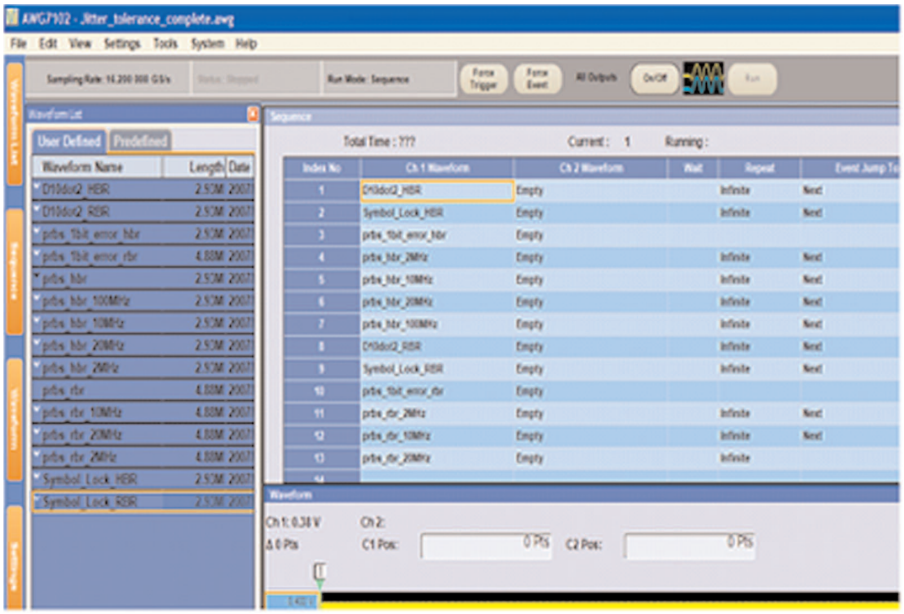


Figure 10. AWG Sequencer mode with DisplayPort Jitter compliance test waveforms loaded.

AWG Markers allow for Crosstalk or Aggressor Lane Testing

The AWG s Marker outputs or Digital Outputs are capable of being used as aggressors for crosstalk testing. DisplayPort requires as part of the Receiver CTS ver 1.0, that if more than one lane is available on the DUT, each lane should be tested with a D24.3 pattern injected on each adjacent lane. Since the AWG7102 has 4 marker outputs, 2 of these outputs can be used for easy adjacent lane testing. See Figure 9.

AWG Sequencer Makes Automation Internal

The AWG's internal sequencer allows for the designer to load all the required waveforms for a specific test and then step through these waveforms as needed. See Figure 10. This enables easy compliance tests where the device needs a transaction signal to be sent prior to the test signal. Using the AWG sequencer allows this without requiring disconnects from one source and reconnects to another. In many cases the transaction signal is a mechanism to put the device in a loopback or test mode and these signals need to be clean or sent without jitter.

Conclusion

High Speed Serial Data Receiver testing is no longer the challenge that it was. With the combination of fast AWG's hardware performance and Direct Synthesis software, this once challenging task has now been simplified. The AWG's sequencer and Marker support allow for full compliance test capability for DisplayPort and is simplified to just a single instrument running a sequence and looking for errors. With this configuration the only limitation is the max data rate available for over sampling of the directly synthesized patterns and your imagination.

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Updated 12 November 2007

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7/08 FL/WOW 76W-21687-1

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