VGA Interface Testing with the VM5000

Many devices depend on high performance color displays, including personal computers, video gaming appliances, and home theaters. Even with digital display interfaces such as DVI, analog RGB persists due to the large number of analog-only displays and the flexibility and reliability of the analog interconnect. Frequently a 15-pin RGBHV analog interface is used. Developed originally for VGA PC graphics cards, this physical interface is capable of very high performance. But impairments can and do occur because of failures or poor design. Verifying proper RGBHV interface operation can help ensure that displays work predictably and deliver top-quality results.

VGA Interface Background

VGA, or Video Graphics Array, is a graphics controller standard introduced by IBM in 1987 with the PS/2 personal computer. Prior to VGA, typical computer displays used simple binary combinations of R, G, and B, sometimes with an added intensity, or I bit. A drawback of the 3-wire binary interface was the limited number of colors and shades of gray that could be reproduced:

8 colors, including black and white, or 16 with the I-bit. By moving to analog representations of the RGB signals, many more intermediate signal values could be conveyed over a 3-wire interface. Standard VGA uses 6 bit representations, allowing 64 independent voltage levels on each of the RGB channels, making 262,144 color combinations possible.

Tektronix

Enabling Innovation

HD-15 VGA Socket
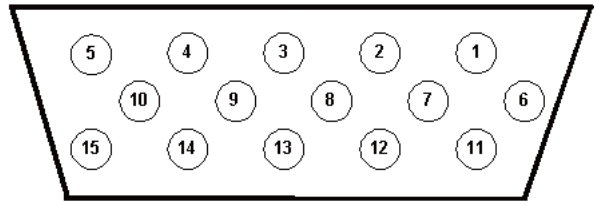
Red out: (+) pin 1, return pin 6
Green out: (+) pin 2, return pin 7
Blue out: (+) pin 3, return pin 8

H Sync out: pin 13, return pin 10
V Sync out: pin 14, return pin 10
Ground: pin 5

Monitor ID: pins 4, 11, 12, 15
Reserved: pin 9

▶ **Figure 1.** *VGA connector pin assignments.*

The VGA physical interface is a RGBHV 5-wire signal, using 700mV analog RGB video levels and TTL-level digital HV synchronization signals. A 15-pin high density D-type connector (HD-15) carries these signals. Figure 1 shows a VGA pin-out. The RGB signal lines are sourced by Digital to Analog Converters (DACs) coupled to video amplifiers capable of driving the 75Ω load assumed by the interface. TTL-compatible logic buffers typically source the HV sync signals.

This physical interface ended up being widely deployed, so it was preserved by subsequent graphics controller designs. Although commonly referred to as "the VGA port," today's 15-pin RGBHV output usually carries display formats with resolutions and color bit depth well beyond that of the 640 x 480 VGA standard.

VGA Interface Performance

The power of an analog RGB interface is its ability to convey virtually any desired video value. In practice, this is limited by noise and distortion. That is, if 6 bit representations are to be carried over the interface, then the noise and distortion level of the RGB signals must be low enough to allow reliable recognition of 64 (2^6) discrete and linearly spaced levels over the full range. If the interface performance does not support this, due to noise, non-linearity, gain errors, or signal transient behavior such as overshoot and ringing, then the potential benefit of higher bit representations is lost.

A more serious consequence of casually extending the VGA interface to higher rates is proper display synchronization. With a larger number of displayed pixels per frame comes a higher horizontal sync frequency, and the need for shorter sync rise times and smaller levels of jitter. Improper detection of the horizontal and vertical sync events can reduce the spatial definition in the image, and at worst result in an unlocked and unrecognizable display.

Parameter	Value
Sync Logic "1"	2.4V – 5.5V @ 8mA source
Sync Logic "0"	0.0V – 0.5V @ 8mA sink
Sync rise/fall time (max)	80% of pixel clock period
Sync monotonic rise/fall voltage range	0.5 – 2.4V
Sync overshoot/undershoot (max)	30%
Hsync jitter p-p (max)	30% of pixel clock period
Video Max Luminance (input=FFh)	700mV + 70mV/-35mV
Video Min Luminance (input=00h)	0.000V
Video rise/fall time (max)	25% of pixel clock period
Video settling time (max)	30% of pixel clock period
Video overshoot/undershoot (max)	12%
Video Integral and Differential Linearity error	±1 LSB
Video channel voltage mismatch (max)	6% over full voltage range
Video channel time skew (max)	50% of pixel clock period
Video Noise Injection Ratio (max)	±2.5% of Max Video Luminance

▶ **Table 1.** *VSIS specification summary.*

VESA Video Signal Standard

The Video Electronics Standards Association (VESA) recognized that performance issues had become more critical as the VGA interface was being applied at higher and higher signal rates. In 1999 VESA released a voluntary standard whose goal was to more tightly define the parameters carried over the RGBHV interface. Called the Video Signal Standard, or VSIS, it provides recommended values for the most important aspects of the RGBHV signal. The VSIS document was subsequently revised in 2000 and 2002.

VSIS makes recommendations in three parts. The first, Synchronization Signal Specification, covers parameters such as sync logic levels, sync jitter, and sync transition behavior. These specs are at the top of the list for ensuring compatibility between two devices connected with the VGA interface. Without proper synchronization, little else matters. The second area, Analog Video Outputs, contains specifications for RGB video levels, noise, and transient behavior. These are the key specifications for ensuring that the analog interface will in fact convey the desired color resolution, whether it is a 6, 8, or 10 bit representation. Finally, the Test Circuits section prescribes the loading at both ends of the interface. Improper loading can substantially alter the transient response for both the sync and RGB video signals.

The VSIS specs are summarized in Table 1. Complete specifications can be found in the VESA Video Signal Standard document, available through VESA (www.vesa.org).

VGA Interface Testing with the VM5000

VGA Test Procedure

In 2002 VESA supplemented VSIS with a companion test procedure. Simply titled "Test Procedure—Evaluation of Analog Display Graphics Subsystems," the document describes recommended methods for measuring VSIS parameters. Twelve tests are detailed, each listing required equipment, test patterns, test procedure, and necessary analysis. If you plan to do VSIS testing, this is an important document. It helps clarify some of the VSIS specifications and their intent.

The VSIS document and companion Test Procedure are both available through VESA. Taken together, they provide an effective approach for assessing VGA interface performance.

Implementing the VESA Tests

The VSIS and Test Procedure are written around an oscilloscope. This is a good fit, given the time-domain nature of many of the specifications. Plus, oscilloscopes are commonly available, and most engineers and technicians know how to operate them. Despite this familiarity, some care must be exercised in selecting an appropriate scope.

First, the scope needs to have an adequate number of inputs. At least two vertical inputs with a separate trigger input are needed. This is to support those measurements that compare two signals; for example, the timing between the R and G video channels. A five channel device, with one input for each of the RGBHV signal lines, would be ideal. This would allow all measurements to take place with one connection.

Second, each signal input needs to provide the appropriate vertical accuracy, sensitivity, and bandwidth for the measurements. The Test Procedure recommends vertical accuracy of ±2% over the 200mV to 1.5V range. It also recommends a minimum -3dB bandwidth of five times the inverse of one pixel time, or five times the Pixel Clock Frequency (PCF). This is to prevent degrading transient response measurements like rise time. With formats that use very short pixel times, this can push the bandwidth requirement to beyond 2 GHz.

Making Connections

Frequently overlooked is the method of connecting the scope to the signal. We want to observe the signal without affecting its characteristics; that is, we want insignificant loading from the scope connection. The 1 MΩ input resistance of most scopes makes this easy at low frequencies. At high frequencies, however, the scope input capacitance begins to dominate. For example, a 20pF input presents an 80Ω reactive load at 100 MHz. This will affect the performance of a 75 Ohm system operating in this frequency range.

VSIS provides clear guidance on test connections and loads. The RGB analog video source is expected to be 75Ω. The test load is specified to be 75Ω, with a tolerance of ±1.5Ω at DC, rising to ±15Ω at 60% of the pixel clock frequency. If the load is predominately a parallel RC, the maximum load capacitance permitted is:

$$Cmax = 1/(377*PCF),$$
where PCF is the pixel clock frequency in Hz

A second consideration is the effect this load capacitance has on the system risetime. The -3dB bandwidth of the interconnect, assuming a 75Ω source and load, is:

$$-3dB\ BW(Hz) = 1/(236*C)$$

Since VESA recommends that the measurement system -3dB point be at least 5X PCF, the maximum C from a bandwidth perspective is:

$$CmaxBW = 1/(1178*PCF),\ with\ PCF\ in\ Hz$$

For example, XGA (1024x768) at 75 Hz uses a 78.75 MHz PCF, so Cmax is 1/(377*78.75 MHz) = 34 pF. CmaxBW is 1/(1178*78.75 MHz) = 11pF. A direct connection to a 20pF scope will meet the VSIS load spec, but will not provide the 5X PCF bandwidth regardless of the scope vertical bandwidth. At higher PCFs the allowed load C is quite small. Display format 2048x1536 at 85 Hz has a nominal 388 MHz PCF, so Cmax = 7pF and CmaxBW = 2pF.
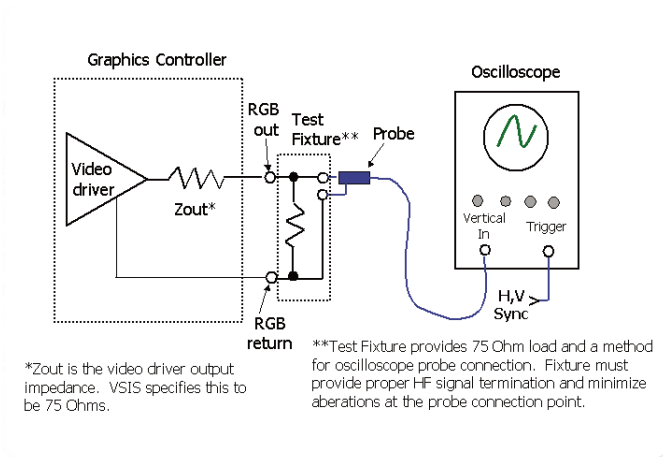
▶ **Figure 2.** *Test connections for RGB measurements.*

▶ **Figure 3.** *VM5000 option VGA system with MIU.*

There are two common solutions to this problem. The first uses voltage probes. Both passive and active variants exist. Often these provide a 10 MΩ load and 10X attenuation. The passive probes usually range between 8 to 15pF at the probe tip, depending on length and design. Most active probes present less than 2pF at the probe tip. For that reason, they are the better choice for PCFs above 50 MHz.

The second measurement approach uses lossy matching. An oscilloscope with a 50Ω input is used, and a min-loss pad is added to the input to create a 75Ω load impedance. Essentially, the oscilloscope 50Ω load is resistively increased or "built out" to 75Ω. This 75 Ohm interface then serves as the test load. Properly implemented, the only limit with this approach is the oscilloscope bandwidth itself.

Irrespective of the method used - voltage probes or lossy matching - great care must be taken in connecting together the signal, test load, and oscilloscope. Common pitfalls are ringing introduced by voltage probe ground leads, and waveform reflections resulting from poor impedance control between the Device Under Test (DUT) signal output and the test load. A custom test fixture, allowing repeatable and controlled interconnect between the DUT, test load, and measurement oscilloscope will produce the best results. See Figure 2.

Automated Testing

Several of the VSIS parameters require a large number of repetitive measurements. For example, Integral and Differential Linearity require 1024 LSB step measurements on each of the three channels of a 10-bit source. Further, multiple format devices like graphics cards may require repeating the test suite for each supported display format. Automating the measurements can substantially cut test time.

Tektronix has developed a measurement package that automates the VESA VSIS tests, the VM5000 Option VGA shown in Figure 3. Based on the Tektronix TDS5104B 1 GHz oscilloscope platform, the VM5000 Option VGA adds signal interface hardware, special signal processing, automatic limit testing, and test stimulus files. In automatic mode, once the display format is selected, the entire VSIS test suite can be run in less than 5 minutes without operator intervention.

VGA Interface Testing with the VM5000
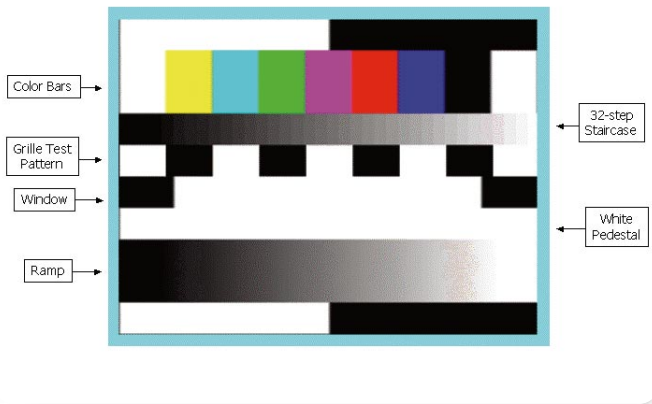▶ Application Note
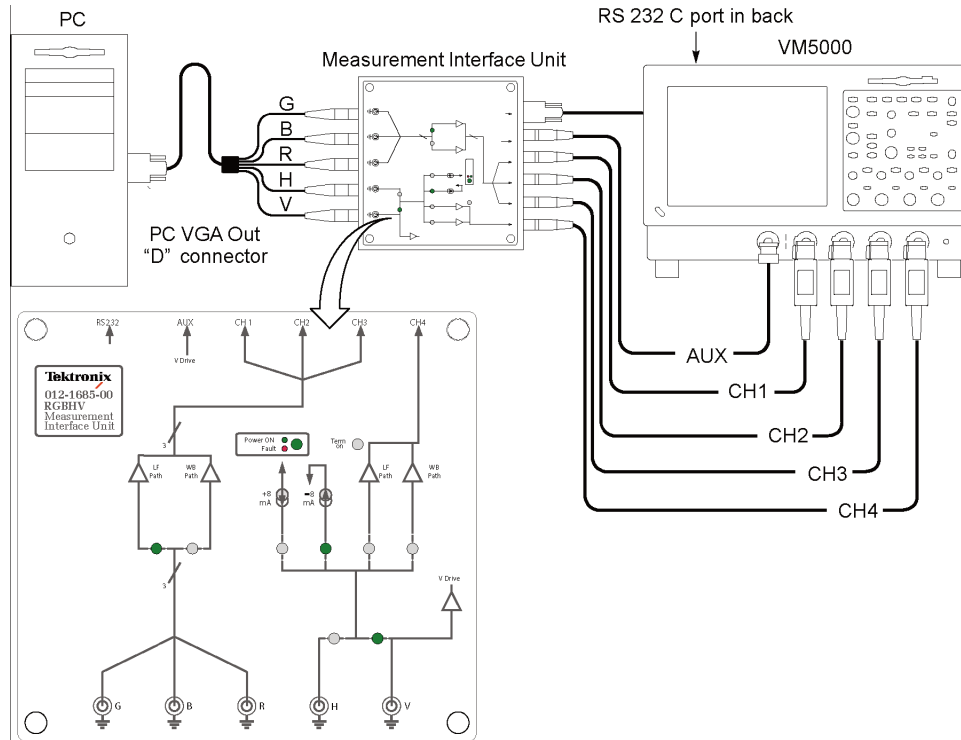
▶ **Figure 4.** *Diagram of VM5000 option VGA test connections.*

Figure 4 shows test connections with the VM5000 Option VGA. An interface pod, called the Measurement Interface Unit (MIU), sits between the DUT and the oscilloscope. The MIU performs several functions:

▶ It provides five fixed inputs, one for each of the RGBHV signals. This allows executing the full VSIS test suite without changing test connections to the DUT. The MIU handles any necessary signal routing under control from the host VM5000.

▶ It provides VSIS compliant test loads. At low frequencies, RGB signals are precision terminated in 0.3% accurate 75Ω loads. When used with the supplied 6 inch HD-15 to BNC adapter cable, better than 21dB Return Loss (RL) at 250 MHz is maintained at the HD-15 pins, supporting up to 416 MHz PCFs (21dB RL corresponds to ±15Ω variation from 75Ω).

▶ It dynamically changes the signal routing and termination method so that both 1 MΩ and 50Ω oscilloscope input modes can be used, depending on the measurement. The 1 MΩ mode is optimum for low frequency amplitude and offset measurements, while the 50Ω mode offers the best high frequency performance.

With the MIU and precision 6 inch adapter cable, no special test fixtures or additional oscilloscope probes are required. Simply plug the adapter cable into the DUT's HD-15 output jack.
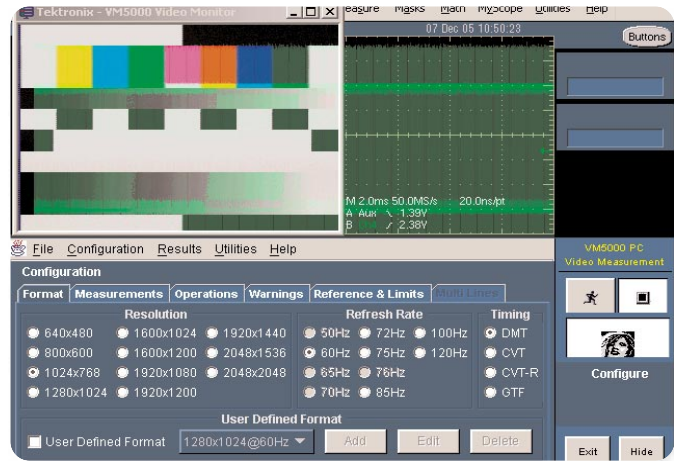
▶ **Figure 5.** *VM5000 option VGA matrix test signal.*

▶ **Figure 6.** *Format configure screen, showing 1024X768 resolution, 60 Hz refresh rate, and DMT timing. Video monitor ON.*

Test Signals

Three static test patterns are recommended for the VSIS measurements. These provide the stimulus for the DUT producing the RGBHV signal. The patterns are:

▶ An alternating black and white vertical striped pattern, called a "vertical grille," made up of 100 pixels on (RGB=FFh) followed by 100 pixels off (RGB=00h) and repeating. The grille pattern is used for RGB video amplitude and transient response measurements.

▶ A gray scale ramp or staircase signal, spanning the range from black to full white across the horizontal. The ramp signal is used for RGB linearity and monotonicity measurements.

▶ A full white flat field or window signal, used for RGB video noise measurements.

In the VM5000 Option VGA, these test patterns are supplied on a CD in all supported formats. Both full field and split field versions are provided. The split field, or matrix test signal, has the advantage that all VSIS tests can be done with just a single test slide. Figure 5 shows the VM5000 matrix test signal. Note that the VM5000 matrix adds additional test patterns, such as color bars, to the recommended VSIS signal set.

Automated Testing with the VM5000

Once DUT test connections are made (Figure 4) and the proper test pattern is being output by the DUT, the next step is to configure the VM5000 Option VGA. A Format Configuration screen (Figure 6) presents several standard choices for Resolution and Refresh Rate. For proper operation, these must match the format the DUT is producing.

The right-most column of the Format Configuration screen, labeled Timing, allows choosing between several VESA display format specifications: DMT, GTF, CVT, and CVT-R[1]. This selection will affect the default test limits that the DUT is evaluated against. In general, older display formats will be governed by DMT, while the most modern formats follow CVT. Reduced blanking devices, like some LCDs, use CVT-R. GTF is used for formats not supported by CVT, such as when the PCF is not an integer multiple of 0.25 MHz. If the Timing standard is unknown, first try DMT. If the selected combination of Resolution and Refresh Rate is not supported by DMT then the instrument will automatically revert to an alternate choice. Again, the VM5000 uses this information primarily for pass/fail limits testing.

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[1] DMT is Display Monitor Timing standard, GTF is Generalized Timing Formula standard, CVT is Coordinated Video Timings standard and CVT-R is Coordinated Video Timings (reduced blanking) standard. All are VESA standards.

VGA Interface Testing with the VM5000

▶ **Application Note**
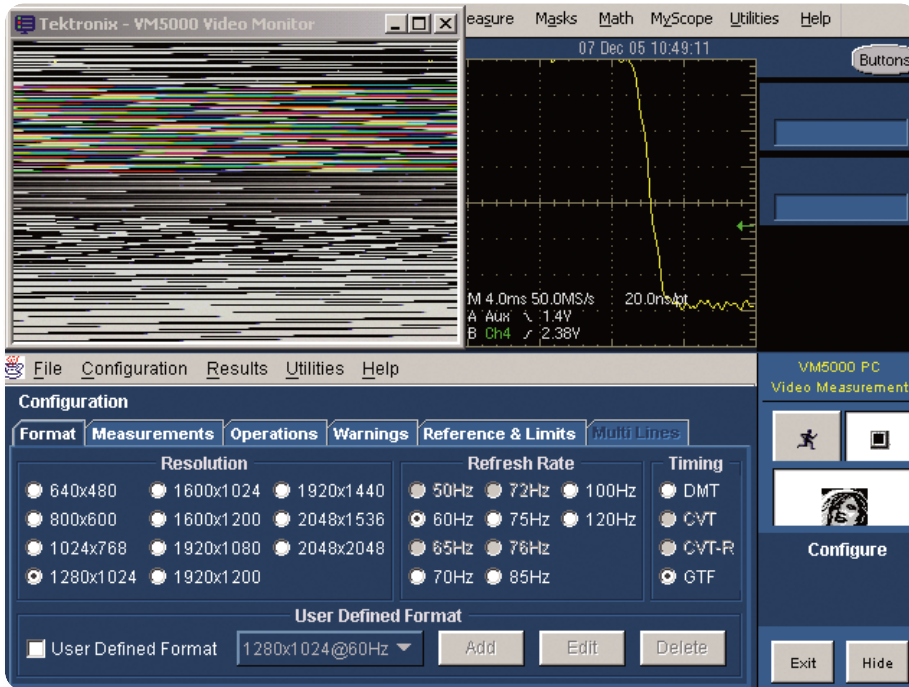
▶ **Figure 7.** *Format configure screen, set for 1280X1024 while receiving a 1024X768 signal, video monitor ON.*
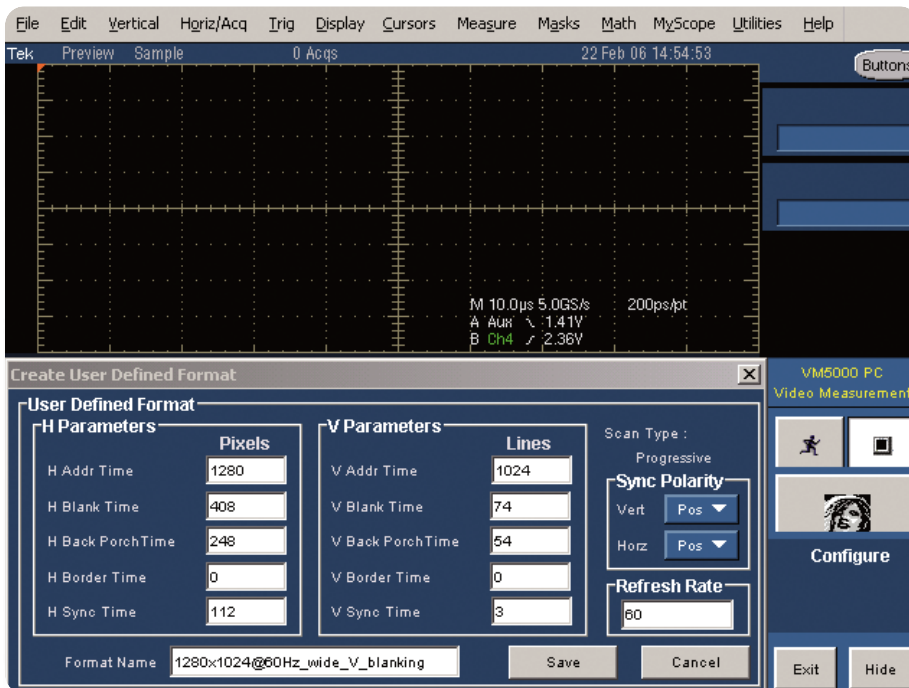
▶ **Figure 8.** *User difined format screen.*

A handy tool for verifying proper configuration is the VM5000 Video Monitor mode. If the DUT output signal and the VM5000 format match, and all connections are correctly made, then a stable picture display showing the test slide will be visible as in Figure 6. With mismatched formats an unlocked display results, such as shown in Figure 7. Video Monitor mode is activated with the large rectangular radio button at the far right of the screen.

Since the VM5000 does depend on the basic horizontal and vertical timing to know where to start and stop measurements, a User Defined Format configuration choice is available for non-standard formats. This is useful for proprietary formats and for troubleshooting malfunctioning standard formats. See Figure 8.

Sync Measurements

Sync measurements evaluate characteristics of the H and V sync pulse signals, their relationship to the RGB video, and jitter. As previously mentioned, these are among the most important VSIS measurements. Display stability and proper picture positioning depend on successful interpretation of sync events. On the VM5000 Option VGA these measurements are organized into five categories: H Sync, V Sync, H Timing, V Timing, and H Sync Jitter.

H and V Sync

H Sync and V Sync measure the sync pulses for amplitude, pulse fidelity, and timing. If these parameters are out of tolerance, then display lock may be unreliable. Figure 9 shows the sync pulse definitions. Figure 10 shows some typical results for a DUT.

For sync measurements, the H and V input ports of the MIU are used. These ports, combined with the special 6 inch HD-15 cable, implement 50Ω transmission lines from the DUT that are terminated differently depending on the parameter being measured:

▶ **Driver Logic Level @ ±8mA.** VSIS specifies the Logic Level "1" (Vmax steady state) to be at least 2.4V while sourcing 8mA. To test this capability, the MIU attaches a current source, which sinks 8mA while the sync signal is in the Logic 1 state. Similarly, to test Logic Level "0" (Vmin steady state), the MIU attaches a current source which sources 8mA while the sync signal is in the Logic 0 state. The current source switching is dynamic, transitioning from one current source to the other over the 1.2V to 1.7V region. No other load is attached.

▶ **Driver Logic Level @ 2.21k.** Instead of the switched current source load, a fixed 2.20 kΩ resistor is attached.

▶ **Rise/fall time, over/under shoot, settling time, pulse timing, and monotonicity.** For these high speed AC characteristics, the transmission lines are terminated in 2.20 kΩ and lossy matching is used with the oscillo-scope in 50Ω mode. Basically, the sync driver in the DUT, which by VSIS is assumed to be 50Ω, sees a short 50Ω line terminated in essentially an open (2.20 kΩ compared to 50Ω). The 50Ω path is well controlled so

that the only substantial reflection is that arising from the open.

The VM5000 test suite incorporates several pulse timin measurements that are not part of VSIS but come from the timing standard for the specific display format. These include sync pulse width, line frequency, field frequency, and PCF. Compliance to these timing specifications is very important for interoperability, since display devices using phase locked oscillators will have a limited synchronization range.

Given the number of parameters evaluated, a good way to approach this testing is to enable Limit Testing, using the VM5000 default values. These limits are computed based upon the Resolution, Refresh Rate, and Timing choices made in the Format menu. Results that are VSIS and monitor timing standard compliant are colored green, and those outside the specifications are red. A red value is not necessarily a problem, but it is cause for closer inspection. In general, 100% "green" results can be expected to produce reliable synchronization.

The VESA Test Procedure method for Sync Logic Level measurement specifies use of a test selected resistor, replacing the 2.2 kΩ load, that will cause 8mA of current flow. This method works for the Logic Level "1" test but with a ground referenced load, will not work for the Logic Level "0" test. The VM5000's use of active current source loads properly tests both logic states.

A noteworthy capability of the VM5000 H Sync and V Sync tests is sync polarity. When in "Auto Detect" mode, the VM5000 can detect and properly lock to either sync positive or sync negative signals, regardless of whether they match the VESA spec for that format. Then, the polarity readouts can be checked for proper sign. Verifying sync polarity is especially important for formats that signal reduced blanking with specific combinations of H and V sync polarity.

H and V Timing

The H Timing and V Timing measurements compare the sync position to the active RGB video, and help establish if the display is properly centered and if the right number of addressable lines are present. Frequently, lines at the top or bottom will be cropped. Figure 11 shows the V Timing Results screen for a 1024 x 768 format. This DUT only has 764 display lines because of improper Top and Bottom Borders. Any information in the top two and bottom two lines will be lost.
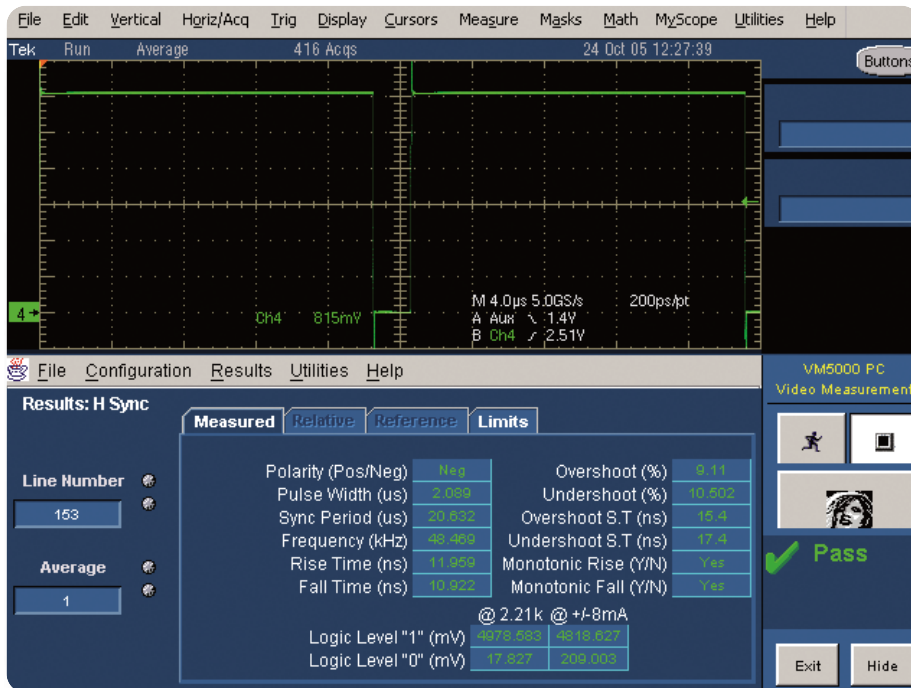
VGA Interface Testing with the VM5000

▶ Application Note
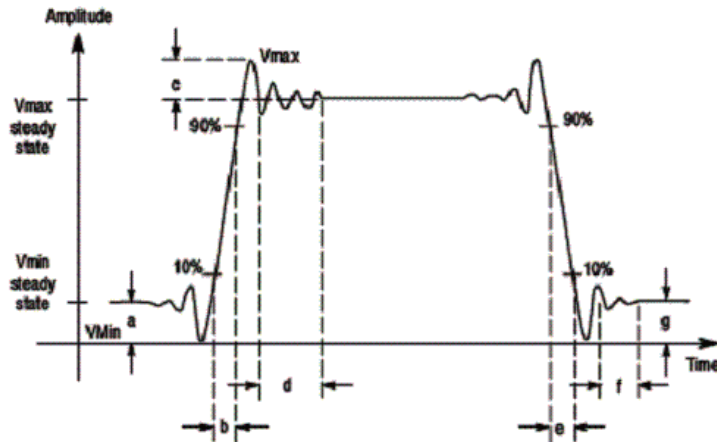
a = Vmin steady state Amplitude (Logic "0" level)
b = Rise Time, 10% to 90% points
c = Overshoot amplitude
d = Overshoot settling time
e = Fall Time, 90% to 10% points
f = Undershoot settling time
g = Undershoot amplitude

▶ **Figure 9.** *Pulse waveform definitions.*

▶ **Figure 10.** *H Sync results screen.*

To use the H and V Timing information to establish picture centering, check that the sum of Bottom/Right Border and Front Porch intervals match the specification for the format in use. These values set the location of the picture bottom and right edges with respect to the V and H retrace points, respectively. See Figure 12.The easiest way to do this is to enable Limit Testing, using the VM5000 Default limits.

▶ **Figure 11.** *V timing results screen.*
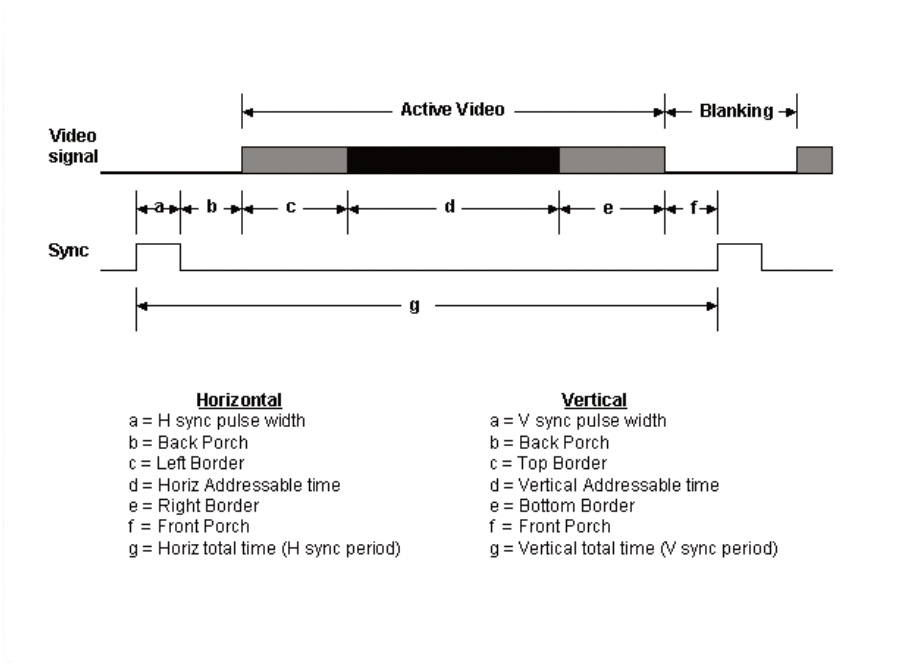
▶ **Figure 12.** *H and V timing definitions.*

H Sync Jitter

The horizontal sync's function is to properly position each line of the display image. Ideally, the time from one H Sync pulse to the next is constant. Should the H sync timing vary, however, parts of the picture within a frame will be shifted horizontally. This sync timing variation is called jitter.

With critical content, shifts of 0.02% of picture width can be noticed. VSIS specifies maximum peak-to-peak H Sync jitter as 30% of a pixel period. This corresponds to 0.047% of picture width for 640 x 480, and 0.015% of picture width for 2048 x 1536.

While a peak-to-peak jitter specification conveniently describes the potential visual effect of jitter on the image, peak-to-peak can be a problem to measure, depending on the nature of the jitter. Some jitter is easily described, especially if it is repeatable and simply correlated to the sync signal. Called Deterministic jitter (Dj), the maximum and minimum peak values are likely to be captured after a relatively small number of measurements. Once this point is reached, additional measurement samples will not produce any change in the reading.

Other jitter arises from disturbances such as random noise and does not have a simple peak bound. Called Random jitter (Rj), it is usually best described by a probability distribution. For Rj caused by typical random noise, the bell-shaped Gaussian distribution is used. Near the center of the bell curve lie the peak-to-peak jitter values that occur most frequently. But there are also very large and small peak values that occur, just not very often. The more measurement samples taken, the higher the likelihood that one of these large or small values will be encountered.

Figure 13 shows the mean peak-to-peak jitter value as a function of the number of measurement samples taken. The jitter is Gaussian-distributed with an RMS value of one. Note that the peak-to-peak jitter value continues to grow as more measurement samples are taken: at 100 samples it is 5.0 while at 1 million samples it is 9.7. Clearly, the number of jitter samples used in a measurement is an important parameter for peak-to-peak jitter when Rj is present.

Figure 13 also shows the uncertainty attached with a peak-to-peak Rj measurement. Although the mean peak-to-peak jitter value increases with the number of measurement samples, the variation in the mean peak-to-peak value decreases. At 100 samples, three standard deviations (3σ) is 36%. This means that if 1,000 different 100-sample measurements are made, 997 (99.7%) will be within a ±36% window about the mean peak-to-peak jitter value. At one million samples, this window decreases to 11%. So, the repeatability of a peak-to-peak Rj jitter measurement improves with the number of samples taken.
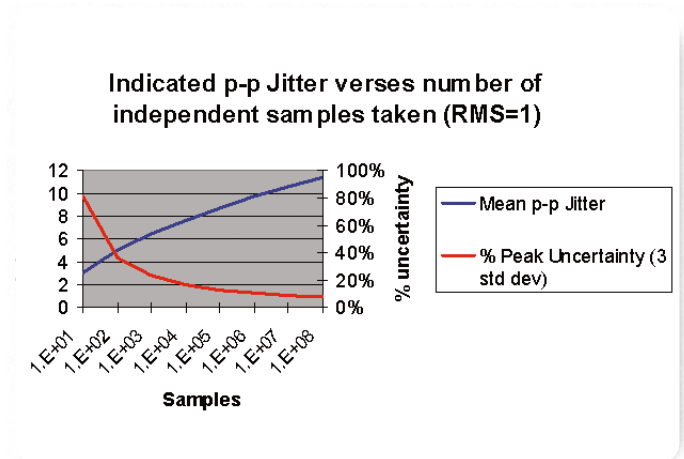
▶ **Figure 13.** *Effect of measurement sample size on indicated peak-to-peak jitter.*

VSIS specifies 100,000 samples for the H Sync jitter measurement. If all of the jitter is Rj, then 99.7% of the measurements will be within ±13% of the mean peak-to-peak jitter value. Typical jitter is a mix of Rj and Dj so the variation will be less than this.

On the VM5000, the user can set the number of jitter samples. Go to the H Sync Jitter Results page and enter the desired value in the "No. of Lines" box. The default value is 100. This allows the measurement to complete quickly, but the jitter result will be low if most of the jitter is Rj. The "No. of Lines" could be set to 100,000 but the measurement time will be very long.

One suggestion is to take a series of 100-sample measurements and compute a mean value. Multiply this mean value by 1.75, which is the ratio of the mean peak values between 100,000 and 100 samples for Gaussian distributed jitter. This gives an estimate of a 100,000 sample measurement if Rj is dominant.

If you are taking a series of jitter measurements on a single DUT, you can reduce the total measurement time by not repeating the system set-up. Perform the first measurement in the normal fashion. Then, in the "Configuration> Operations" menu, select "Run Only." This saves about 15 seconds per measurement. Return the setting to "Setup & Run" before moving to a new device or measurement.

Video Measurements

Video measurements evaluate characteristics of the analog RGB signals, including levels, transient behavior, and noise. Assuming proper synchronization, the RGB video performance will determine display fidelity. On the VM5000 Option VGA these measurements are organized into seven categories: Luma Levels, Color Bars, Ch-Ch Mismatch, Video Transient, Linearity, Ch-Ch Skew, and Noise Injection Ratio.

Luma Levels

The Luma Levels measurement assesses the RGB voltage levels when full white (value FFh) and black (value 00h) images are being output. Proper levels are important for correct brightness and contrast at the display. Ideally, white level will be 700mV and black will be 0mV. These are absolute measurements, using the RGB signal return lines as a reference. The "Vertical Grille" test pattern is used.

At the MIU, the RGB signals can be routed through one of two paths: either "Low Frequency" (LF) or "Wideband" (WB). For Luma Levels, the LF path is used. In LF mode, each channel is terminated in a precision (0.3%) 75Ω resistor before being sent over 50Ω coax pigtails to CH1-3 of the VM5000. Note that the signal ordering is: G to CH1, B to CH2, and R to CH3. Each scope channel is DC coupled and set to 1 MΩ termination. This produces the highest DC measurement accuracy since the scope has its best sensitivity and S/N ratio in this configuration, and the 75Ω termination accuracy is set by the single 75Ω precision resistor in the MIU. The three 50Ω coax pigtails are source terminated within the MIU, to absorb reflections from the open (1 MΩ) ends at the scope.

To reduce errors arising from oscilloscope voltage offset, each scope input channel is first set to "GND" coupling and measured. Then, with the coupling restored to "DC," measurements are taken of the white and black levels from the DUT. The "GND" value is subtracted from the DUT measured values before reporting the results.

VSIS specifies the white level as 700mV +70mV/-35mV. Black is specified as 0mV, with no tolerance given. The VM5000 uses a default black tolerance value of +70mV/-35mV. Since overall black level can be adjusted at the display using the Brightness or Black Level control, this is not too critical.

Color Bars

The Color Bars measurement comes from the Video industry. While not a VSIS specification, it has attributes that make it useful for the RGBHV interface. Color Bars shows the RGB voltage levels for the eight different white/black RGB combinations. For example, Red is R=700mV, G=0mV, B=0mV; Yellow is R=700mV, G=700mV, B=0mV; White is R=G=B=700mV. In all, 24 voltage measurements are made for the eight colors. A Color Bar test pattern is used. The MIU is set to LF mode for Color Bars.

Color Bars are a good way to see that the RGB signals behave properly when various combinations are active. For example, is the R signal affected by G being on or off? Comparing the Yellow and Red bar values shows this. Also, since the bars are uniquely identifiable across the line (as opposed to the Vertical Grille pattern), line tilt can often be observed. Ideally, the White, Yellow, Cyan, and Green bars should all produce the same G signal value, nominally 700mV. If G starts out at 700mV, but drifts down in value over the next three bars, there may be tilt in the G channel.

Color Bars uses the RGB signal horizontal Back Porches as the 0V references. Horizontal Back Porch is the video signal region between the end of H sync and the start of the Left Border (see Figure 12) that maintains a level representing the video black voltage. By sampling this voltage and using it as the 0V reference, any voltage offset in the video channel is ignored by the Color Bars measurement. Also, absolute offset error in the VM5000 is ignored for the same reason. This is in contrast to the Luma Levels measurement which references not to the signal Back Porches but to the signal return lines. Since most display devices use the Back Porch to set the black point, Back Porch referenced measurements usually correlate better to perceptual picture performance, especially for RGB values near black.

Color Bars should produce signal levels similar to that in Luma Levels. If the black values are substantially different between the two measurements, this likely indicates voltage offset in the affected channel(s).

The VM5000 does not require any specific order to the bar pattern, other than that the first bar be white and that a similar white bar be last. This allows non-standard patterns to be successfully used, but also means that this measurement cannot reliably indicate if the RGB channel connections are swapped.

Ch-Ch Mismatch

Ch-Ch Mismatch compares amplitude matching between the RGB channels. In the VM5000, checks are made at 32 equally spaced levels between Black (00h) and White (FFh), using a staircase test signal. For each step of the staircase, the RGB voltages are measured relative to the channel Back Porches. The voltages are then compared: G to B, G to R, and B to R. The largest error in the 32 measurements is reported, for each of the three comparisons. The MIU LF mode is used.

This is an important measurement, for accurate gray scale reproduction is far more dependent on inter-channel amplitude matching than on absolute channel level. This measurement is not affected by offset since it is Back Porch referenced.

VSIS specifies the maximum matching error to be 6% of Vmax steady state. In the VM5000, Vmax steady state is the measured white value, nominally 700mV. So, a maximum of 42mV matching error is allowed. Note that, for a 32 step staircase spanning 700mV, this corresponds to approximately two steps of difference.

VSIS aside, the tolerable amount of channel mismatch is very application dependent. Variables such as reproducer gamma characteristic, ambient lighting, reproducer brightness and contrast settings, and the content itself will affect the viewable threshold. One suggestion is to view the test slide on the destination reproducer, and note how visible the individual 32 step staircase levels are. Regions where individual stairstep boundaries can be seen may benefit from 3% or better matching.

Video Transient

Video Transient evaluates the fidelity of black-to-white transitions of the RGB channels. The Vertical Grille test pattern is used, transitioning from black to white in one pixel time. Each channel is measured for 10 – 90% rise and fall time, overshoot (positive transitions), undershoot (negative transitions), and settling time.

For any picture that has fine detail or sharp boundary changes, adequate transient response is very important. Slow rise or fall times, for example, will show as blurred or indistinct picture changes. Excessive ringing will show as alternating light/dark changes to the picture material following the transition. Over and Undershoot are less of a problem, unless the transition takes a long time to settle.

In fact, some over/undershoot can enhance the perception of transition sharpness. Many display devices intentionally introduce controlled pre-shoot and overshoot, a process known as Aperture Correction.

For Video Transient measurements, proper DUT connection is vital. The VM5000 system provides a special 6 inch VGA-to-BNC cable to attach the DUT to the MIU. The RGB conductors are high quality 75Ω coax with 75Ω connectors, and the overall length is kept as short as possible. Using this cable with the MIU will provide proper return loss and known bandwidth at the VGA port for the RGB channels. Further, the minor linear distortions contributed by this cable and the MIU pigtails have been compensated for by correction networks internal to the MIU. If other cables are used, the high speed measurement results may not be accurate. The 6 inch cable is designed as a field replaceable assembly, so that when the HD-15 connector becomes worn from repeated use a new cable can simply be substituted.

For these measurements the MIU is set to WB mode, implementing a wideband 75 to 50Ω lossy match that then feeds the oscilloscope 50Ω input. This configuration provides the best bandwidth and high-frequency 75Ω DUT termination. All of the Video Transient measurements are relative measurements, so absolute amplitude accuracy is not important.

Video Transient requires flat frequency response to beyond 1GHz, in order to measure the very highest PCF formats. The VM5000 system with MIU has a nominal system rise time of 400ps, approximately corresponding to a 1 GHz -3dB bandwidth. Reported rise and fall time measurement results are corrected for the 400ps system, using the formula:

$$tr(result) = \sqrt{tr(measured)^2 - tr(system)^2}$$

This allows 450ps rise time measurements with better than 20% accuracy.

VSIS specifies rise and fall times to be no greater than 25% of the pixel clock period. This means, quite appropriately, that shorter rise/fall times are needed as the PCF increases. For example, 1024 x 768 at 60 Hz has a PCF of 65.0 MHz, so the maximum rise/fall time is 3.85ns, while for 2048 x 2048 at 60 Hz the PCF is 360.1 MHz and the maximum rise/fall time is 694ps. For devices that can output more than one format, make sure that the highest PCF format is tested.
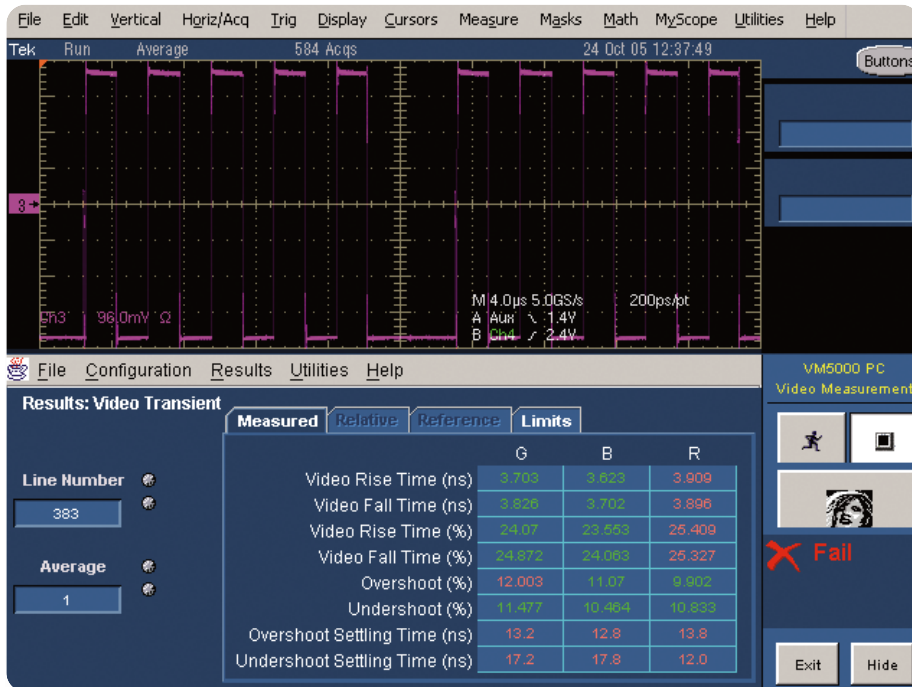
▶ **Figure 14.** *Video transient results screen.*

Figure 14 shows Video Transient results for a DUT outputting 1024 x 768 at 60 Hz. The red channel is slightly failing the VSIS rise and fall time specifications. All three channels substantially exceed the 4.6ns settling time spec (30% of the 15.4ns pixel clock period).

Settling time can be tricky to measure. The decay from the initial overshoot transient is usually exponential, often with damped ringing. VSIS considers the transition settled when it reaches 5% of the full scale value. Sometimes two adjacent peaks of the damped ring will be near the 5% threshold. In this case, noise can cause the settling time result to jump back and forth between two values. Note that a waveform with less than 5% overshoot will show 0ns settling time since the 5% threshold is never reached.

Linearity

Linearity checks how the DUT behaves between the black and white points. Ideally, if a constant slope ramp is applied to the input, a constant slope ramp will be reproduced at the DUT output. Typically, the output ramp will show some slope variation. This variation is linearity error.

Linearity is important for proper gray scale rendition. For example, compression (slope decreasing) may lead to an input gray level transition having reduced contrast at the output. Also, if there are substantial linearity differences between the individual RGB channels, a black-to-white gray scale pattern may end up appearing slightly colored in places.

VSIS defines two types of linearity measurements. The first, Integral Non-Linearity (INL), checks the overall slope error between black and some other point. The second, Differential Non-Linearity (DNL), evaluates slope error between two adjacent points. In both cases, the test signal is a black to white ramp. Virtually all modern graphics systems internally use digital representations. Thus, our constant slope ramp will be in reality a series of steps. A system using 8 bit representations will have 256 steps; a 10 bit system will have 1024 steps. A DAC converts these digital representations to the analog signal that appears at the DUT output. INL and DNL measurements are then made at each step location.

VGA Interface Testing with the VM5000

The first task is to determine the number of steps and their location in the DUT output signal. This can be difficult, particularly for 10 bit systems. With 1023 transitions between 0V black and 700mV white, each transition, or LSB, is only 0.7mV. Between noise, distortion, and clock crosstalk in the DUT, and noise in the measurement oscilloscope, a 0.7mV signal may not be easily recognized. To accomplish this, the VM5000 first takes 500 separate waveform acquisitions that are averaged. This reduces the random noise and quantization error. The start and end of the staircase are identified, and then a linear ramp is subtracted from the signal. This leaves a sawtooth waveform, still containing noise and distortion. The fundamental frequency of this waveform is determined and used to set up a corresponding mask filter to pass the fundamental and selected harmonics. The mask filter is then applied to the sawtooth signal, producing a signal with better defined transitions. By counting the mask-filtered sawtooth transitions, the number of steps can be determined. These transitions also locate the start and stop of individual steps of the original staircase signal, and are used to gate a series of mean level measurements by the oscilloscope. A measurement is taken for each identified step.

A series of calculations are then made:

▶ Ideal LSB value: LSBc = [Vout(N-1) - Vout(0)]/(N-1), where N is the total number of identified steps;

▶ INL at step n: INL(n) = [V(n)-LSBc*n]/LSBc

▶ DNL at step n: DNL(n) = [V(n) - V(n-1)]/LSBc

▶ Resolution: bits = log(base 2)[N]

The units for both INL and DNL are LSBs.

The VM5000 will report the maximum INL and DNL, and identify the step location where they occur. It will also verify that all step values increase monotonically. Sometimes, if many steps are similar, noise will cause different step numbers to be identified each time the measurement is run. This simply indicates that there is no single step that dominates non-linearity.

VSIS specifies that INL and DNL should not exceed ±1 LSB and that a monotonically increasing test ramp produce monotonically increasing RGB voltage values.

Sometimes, one or more of the bits in a digital word will be frozen or "stuck". When called upon to produce a constant positive-slope ramp, the stuck bit will cause the ramp to increase in an irregular and non-monotonic fashion. This will provoke high INL and DNL readings and monotonicity errors. If stuck bits are suspected, use the oscilloscope window to observe the ramp. The periodicity of the error can often be seen and can identify the bit: a divide-by-2 pattern points to the MSB, divide-by-4 the MSB-1, etc. Note that a stuck LSB will not show up in this manner, but rather as reduced resolution. For example, a 10-bit system with a stuck LSB will be detected as 9 bit resolution, with INL and DNL values commensurate for 9 bits.

Ch-Ch Skew

Channel-to-Channel skew measures the time alignment of the RGB component channels. If they are not aligned, then RGB signal transitions will not occur at the same point on the display. A black-to white transition, for example, might have a narrow red border if the B and G channels are delayed relative to R. As with H Sync Jitter, relatively small amounts of shift can be noticed. VSIS specifies a maximum time shift of 50% of the pixel clock period between any two components.

The VM5000 makes this measurement using correlation techniques. A pair of channels are sampled, using sync as the datum. Then, the interpolated data sets are shifted and compared. If the two data sets are very similar, sample for sample, a high correlation coefficient is attached to this specific alignment. If they are not similar, then the correlation coefficient is small. This process is repeated for a range of positive and negative sample offsets. The offset that produces highest correlation is the time skew for the two channels.

The correlation technique has two main advantages. First, it can use a variety of test signals—step transitions, sine wave burst packets, even picture material—as long as there is sufficient mid and high frequency content. Second, random noise is reduced by the averaging effect of multi-point correlation.

Noise Injection Ratio

This is a measure of noise in the individual RGB channels. VSIS specifies a peak-peak noise measurement on a white pattern, made over a 500 MHz bandwidth. The peak-peak noise value should not exceed 5% of the white voltage, nominally 700mV.

Like jitter, noise may consist of both deterministic and random components. The random components present the same peak-to-peak measurement problem as they did for H Sync jitter. That is, the mean peak noise value will increase with the number of samples taken, while the variation in the mean peak value decreases as the sample size grows. Particularly with wideband, high PCF formats, the random noise term will likely be dominant. So it is important to specify the noise measurement sample size if peak-to-peak results are to be comparable.

VSIS specifies 100,000 noise samples over a 2 second measurement interval. The VM5000 takes 100,000 samples, on each of the three video channels. A user may choose to perform a running average on multiple 100,000 sample acquisitions, by changing the "Average" setting in the "Noise Inj Ratio" Results window. More averages reduce the measurement uncertainty in exchange for increased measurement time. Since a running average is used, the user can choose to stop the measurement early if the results have reached the desired stability. The VM5000 normally uses a 500 MHz noise measurement bandwidth. This can be defeated by de-selecting the filter in the "Noise Inj Ratio" Results window.

To extend the noise measurement range, the VM5000 subtracts its noise floor from the measured result. Prior to measuring the DUT, the VM5000 switches to "GND" coupling and makes a 100,000 sample measurement on each channel. Then the VM5000 reverts to "DC" coupling and the DUT is measured. The two sample record mean square values are subtracted, and the result is converted to a mean peak voltage. The cancellation is not perfect but does extend the measurement range below the noise floor of the scope.

VGA Interface Testing with the VM5000
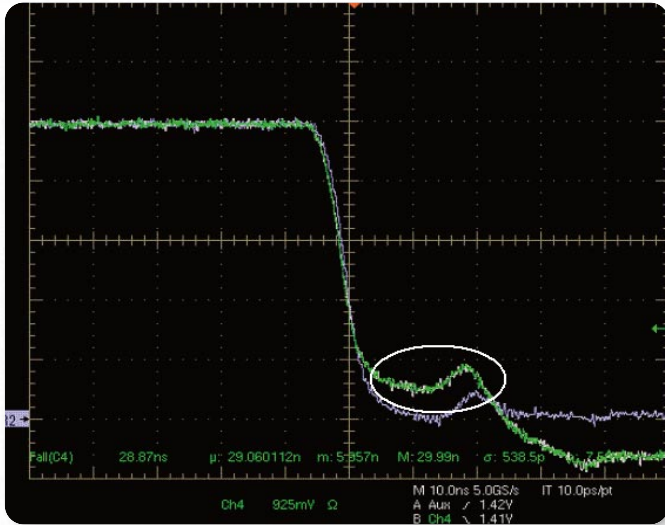
▶ Application Note

▶ **Figure 15.** *DUT with non-monotonic sync.*

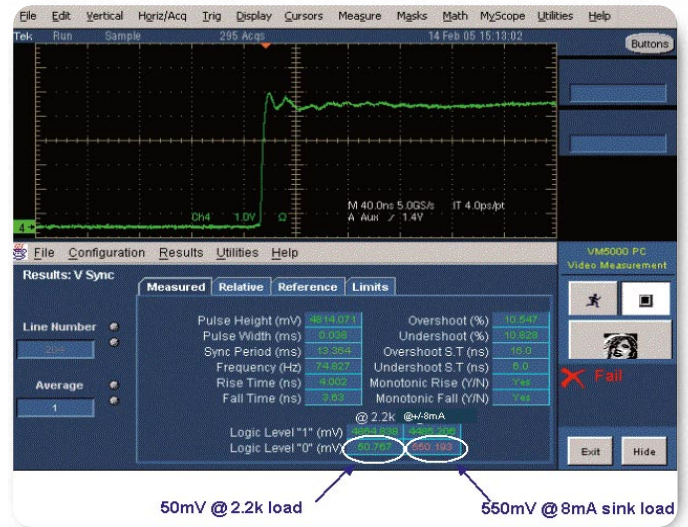▶ **Figure 16.** *DUT with non-compliant logic "0" level.*

What Matters Most

With all the parameters that VSIS evaluates, it's natural to wonder which items are the *really* important ones. The answer varies, depending on the application and what is most important to the user. So here is some guidance for you to determine your own priority.

If interchange—the ability for a source to work with a variety of display devices—is most important, concentrate on H and V Sync measurements, RGB Luma Levels, and Color Bars. These help establish that proper synchronization will occur, that white/black levels are correct, and that the RGB signals are all active. For the Sync measurements, especially watch for these impairments:

▶ Incorrect Polarity

▶ Frequency error

▶ Excessive Over/Undershoot (especially excursions entering the 0.5-2.4V range)

▶ Non-monotonic Rise or Fall

▶ Logic Level "0" and "1" out of spec when driving 8mA loads

Figure 15 shows a non-monotonic sync transition, illustrating slope reversal in the 1.2V region. This could confuse display monitor trigger circuits and cause display jitter. Figure 16 shows a sync Logic Level "0" that pulls only to 550mV when sinking 8mA. While this will likely still work (spec is 500mV max), the substantial difference between the 50mV Logic "0" voltage with a 2.2 kΩ load and the voltage with the 8mA load suggests marginal drive capability, especially if a capacitive load is encountered.

If display system gray scale performance is very important, for applications like color matching, concentrate on Channel-to-Channel (amplitude) mismatch, Linearity, and RGB Luma Levels measurements. Ch-Ch Mismatch will provide information on how closely the channels are tracking each other throughout the video range. Linearity provides a closer look at each channel's black to white transfer function. RGB Luma Levels verifies if the entire 700mV video range is being used, important for proper image contrast.

Picture rendering applications, such as PC video, will benefit from focus on Noise, Transient Response, RGB Luma Levels, Channel Matching (both amplitude and time skew), and H-sync Jitter. Note that motion-related picture artifacts will not be stimulated and detected by the VSIS tests. But, picture images with lower levels of random noise and jitter will typically have lower artifact levels when passed though compression.

For VSIS compliance testing, run the entire measurement suite. Color Bars can be omitted since it is not part of the VSIS specification. For a true compliance test, run the H Sync Jitter measurement at 100,000 lines. Use the VM5000 report generator to produce a secure summary of the test results.

The combination of VSIS and the display timing standards involve a great many parameters. Do not be surprised if your DUT measures out of specification in a few areas. Rather, examine the failures to determine if they are important in your application.

Summary

The 15-pin RGBHV analog interface, commonly known as VGA, is capable of very high performance. As an analog interface, however, it is prone to a variety of impairments, especially when carrying high bandwidth formats. The VESA VSIS specification provides a guideline for measuring these impairments and defining acceptable performance. If designers of both sources and display devices follow the specification, interchange is virtually assured and high fidelity images should result.

One problem has been the lengthy nature of full VSIS compliance testing. Now, with the Tektronix VM5000 Option VGA, these measurements can be made quickly and simply. In addition to automating the test suite, Tektronix has addressed many subtle points of the VSIS measurements so that consistent and accurate test results are obtained. By supplying a complete measurement system, including test signal files, interface accessories, and pre-programmed limit testing, test variations are minimized and results between test systems can be compared. Warranted performance specifications allow compliance testing to be performed without worrying about measurement accuracy questions.

The VM5000 can be used in a variety of ways, from a fully automated pass/fail tester to a manually operated in-depth troubleshooting tool. The ability to override and modify default measurement configurations makes it a useful tool for the R&D engineer. Hopefully, this Application Note has improved your insight on the VSIS measurements and how to effectively use the VM5000 to ensure proper VGA interface performance.

Contact Tektronix:

For Further Information

Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

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