Introduction to Synchronisation

Synchronous versus Asynchronous

Traditionally, transmission systems have been asynchronous, with each terminal in the network running on its own recovered clock timing. In digital transmission, "timing" is one of the most fundamental operations.

Since these clocks are not synchronised, large variations can occur in the clock rate and thus the signal bit rate. For example, an E3 signal specified at 34 Mbit/s ±20 ppm (parts per million) can produce a timing difference of up to 1789 bit/s between one incoming E3 signal and another.

Asynchronous multiplexing uses multiple stages. Signals such as asynchronous E1s (2 Mbit/s) are multiplexed (bit-interleaving), extra bits are added (bit-stuffing) to account for the timing variations of each individual stream and are combined with other bits (framing bits) to form an E2 (8 Mbit/s) stream. Bit-interleaving and bit-stuffing is used again to multiplex up to E3 (34 Mbit/s). The E1s are neither visible nor accessible within an E3 frame. E3s are multiplexed up to higher rates in the same manner. At the higher asynchronous rate, they cannot be accessed without demultiplexing.

In a synchronous system, such as SDH, the average frequency of all clocks in the system is the same. Every slave clock can be traced back to a highly stable reference clock. Thus, the STM-1 rate remains at a nominal 155.52 Mbit/s, allowing many synchronous STM-1 signals to be multiplexed without any bit-stuffing. Thus, the STM-1s are easily accessed at a higher STM-N rate.

Low-speed synchronous virtual container (VC) signals are also simple to interleave and transport at higher rates. At low speeds, 2.048 Mbit/s E1 signals are transported within synchronous VC-12 signals which run at a constant rate of 2.304 Mbit/s. Single-step multiplexing up to STM-1 requires no bit-stuffing and VCs are easily accessed.

A mechanism known as "pointers," operating in conjunction with buffers, accommodates differences in the reference source frequencies and phase wander, and so prevents data loss during synchronisation failures. This is discussed in more detail later in this primer.

Synchronisation Hierarchy

Digital switches and digital cross-connect systems are commonly employed in the digital network synchronisation hierarchy. The network is organized with a master-slave relationship with clocks of the higher-level nodes feeding timing signals to clocks of the lower-level nodes. All nodes can be traced up to a Primary Reference Clock (PRC).

Synchronising SDH

The internal clock of an SDH terminal may derive its timing signal from a Synchronisation Supply Unit (SSU) used by switching systems and other equipment. Thus, this terminal can serve as a master for other SDH nodes, providing timing on its outgoing STM-N signal. Other SDH nodes will operate in a slave mode with their internal clocks timed by the incoming STM-N signal. Present standards specify that an SDH network must ultimately be able to derive its timing from a PRC.

Evolution of Timing and Synchronisation

This is a time of great change for Timing and Synchronisation in the network and there are many challenges for operators and suppliers – and many issues to resolve:

- Synchronisation networks are changing with the introduction of SDH; the historical PDH-based sync network will be replaced by an SDH-based architecture.
- New equipment, network timing, and sync standards have been developed (Tektronix is contributing expertise at ITU and ETSI).
- Transport networks are evolving and hybrid SDH/PDH has specific problems due to the quantisation of network phase variation as pointer justifications.
- New services such as video and ATM depend on excellent timing and network sync to deliver good Quality of Service.
- Jitter/Wander measurement technology is changing from analogue to digital, leading to dramatically new instrument capabilities.
- New test equipment standards are being developed (Tektronix is taking a leading role at ITU).

These and many other timing and sync issues are addressed in another publication from Tektronix: ***Performance Assessment of Timing and Synchronisation in Broadband Networks.*** Copies can be requested from Tektronix offices or by visiting www.tektronix.com.